Elimination Of ESD Defects using DICO2

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FLASH FORWARD

Introduction

- Fab25 – Spansion's 8 inch wafer NOR Flash memory Fab, Austin Tx
- Fab25 has been undergoing conversion from an 130/110 nm Aluminum back-end to 90/65 nm Copper damascene process over the last 2 years
- Shifted from Floating Gate to Spansion MirrorBit technology
- As we 'climbed' the yield improvement ladder new signals were identified including a donut pattern of yield loss in the region near the center of wafer
- Collaborative investigation with SEZ America and Qcept Technologies provided opportunity for rapid learning

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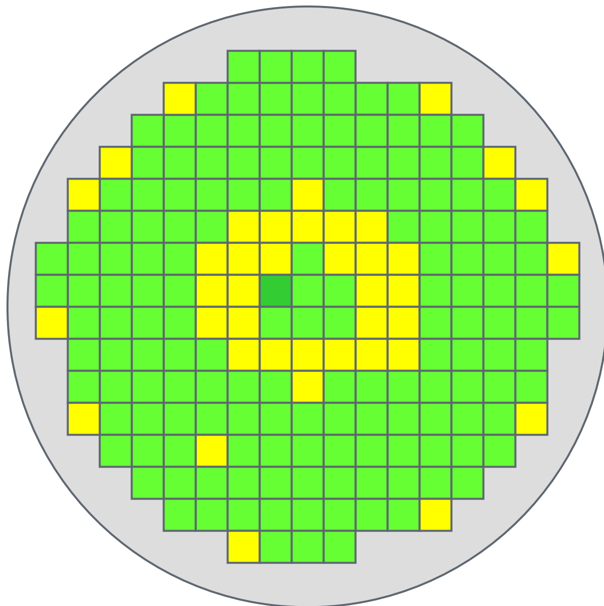
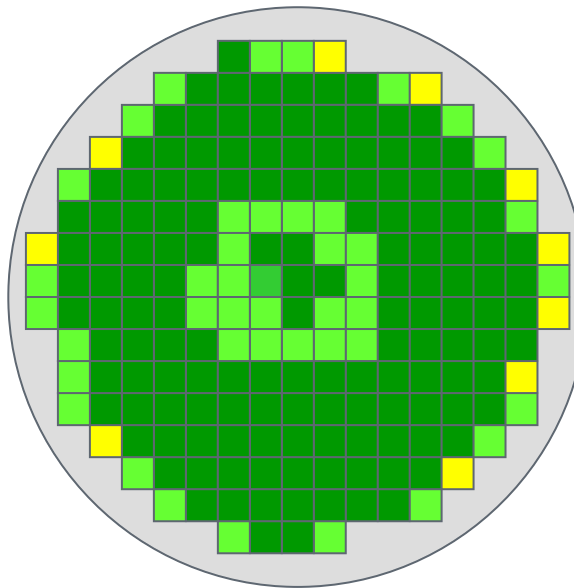
Relative Yield Analysis – Composite Wafer Maps

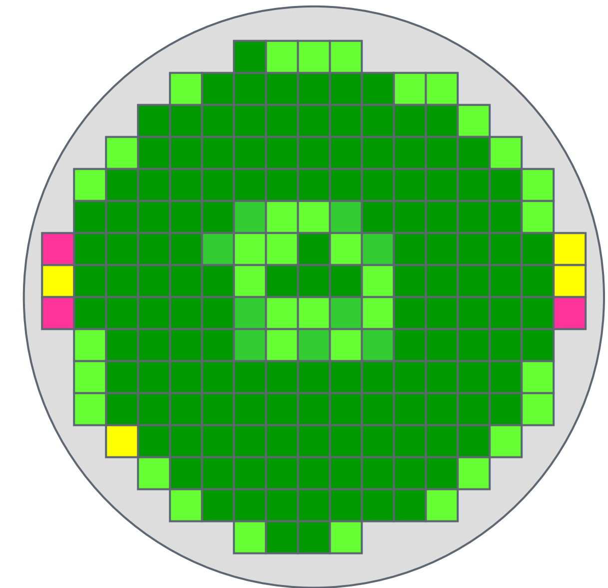
Product A



Product B



Product C



-Stacked wafer maps (~100 wafers) identify center donut region with reduced yield

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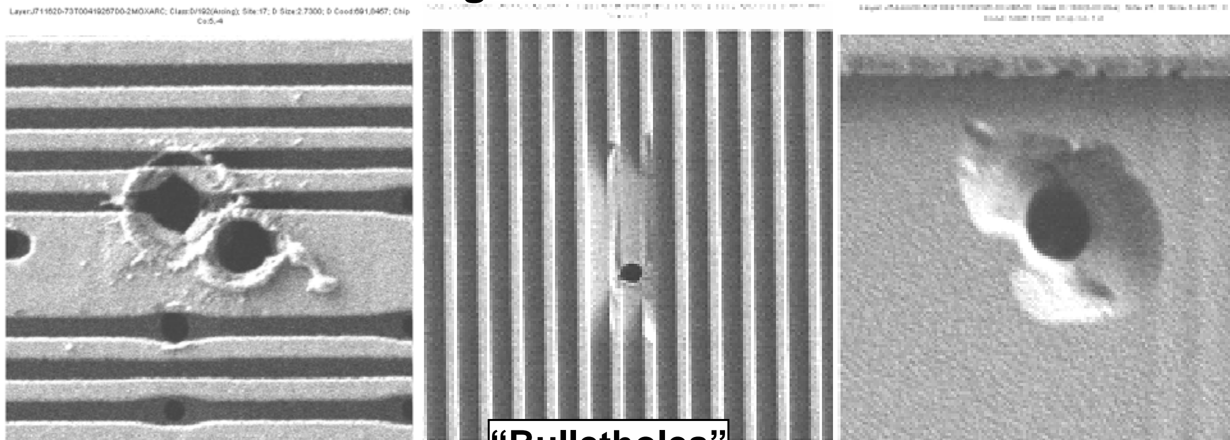
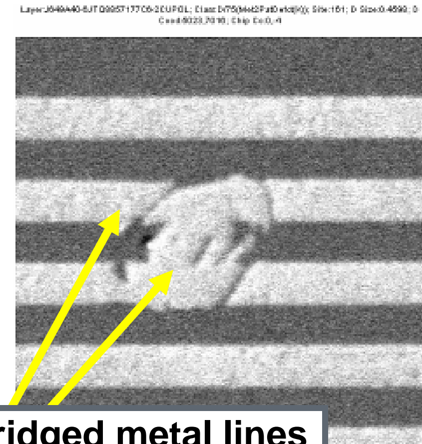
Inline Defect Review

- A Defect-to-Sort correlation on defective die in the donut region identified defects that correlate with specific SORT bin failures
- This defect type is found/observed in the center of the wafer and not out near the edge, consistent with the SORT signal
- The defect morphology is consistent with micro-arcing, typically from the trench etch process
- Significant effort invested in trench etch recipe modifications to quantify and reduce arcing without positive effect

Defect Images Post- Trench Etch



Post- Cu Polish



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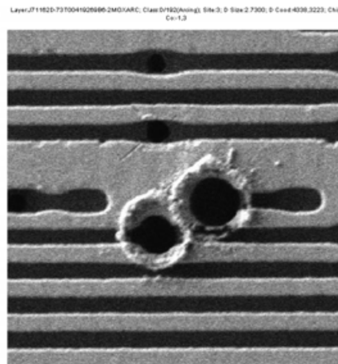
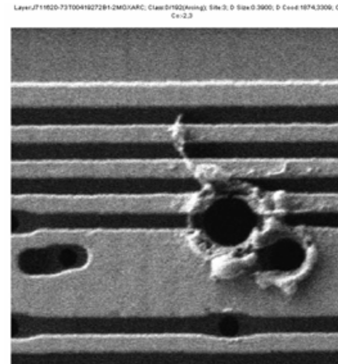
What Process Step Causes Arcing?

- Arc defects prior to WS indicates arcing occurs in Trench Etch process
- One arc defect detected post-WS, not detected in pre-WS scan
  - A new defect or one missed by pre-scan?

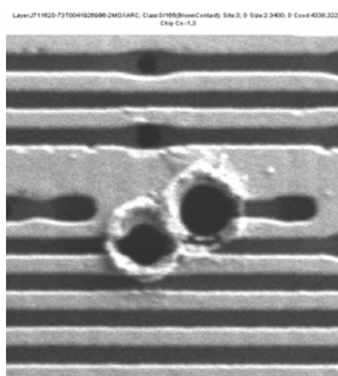
Pre WS

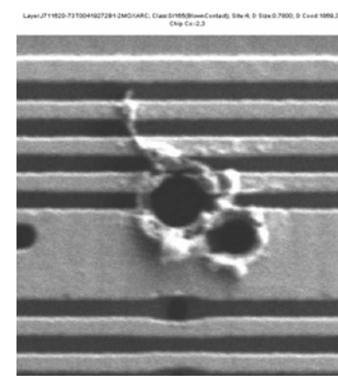


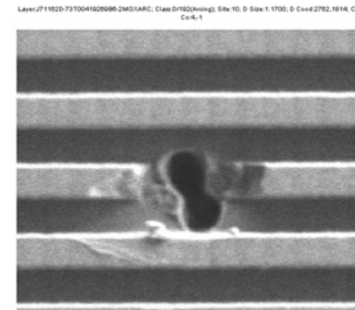


No defect present in pre-scan

Post WS







New Defect?

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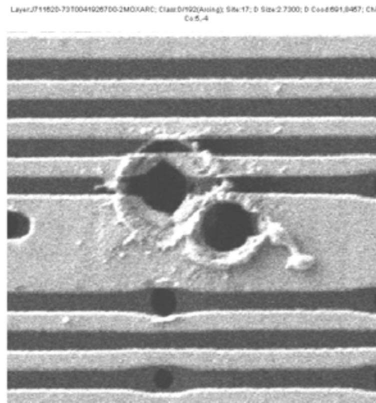
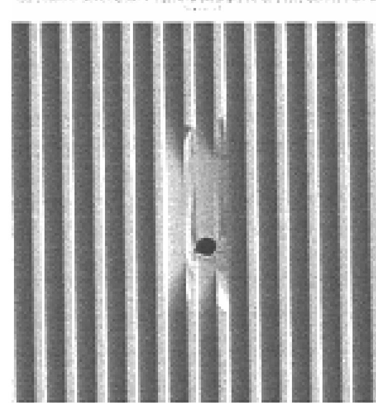
Evaluation of Wet Strip Tool Contribution to Arcing

- An extensive analysis of Wet Strip (WS) tool contribution to arc defect generation was conducted using product wafer scans 'tuned' to improve arc detection
  - Difficult as arcing is a low frequency event
  - Multiple wafers scanned post-etch/pre-WS, and then after iterative runs on the WS process
  - # Arc defects detected increased with sequential WS processing
  - Distinct arc defect morphology difference noted between typical Etcher induced arcs and SEZ WS arcs
- 'Scoring' of historical defect images suggested > 85% of arcs were created in WS portion of process flow!

Typical Etcher Defect
- Frequently 'double strike'
- Ring of material around hole
- Melted appearance





Typical WS Defect
- Always single site
- Oxide missing/sheared
- Very clean, no slag

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How/Where Does Arcing Occur in a Wet Tool?

- WS process conducted on SEZ single wafer spin processor(s)
- Use of a conductive media (DHF), implicates portions of the process where no conductive material is present for arc generation
  - Tool environment, wafer handling, DI rinse, N2 Dry, etc.
- A number of tool and environmental parameters were investigated in collaboration with SEZ America

• Ion Bar setup	• Light
• Spin speed	• Media delivery materials/ grounding
• DI water resistivity	• Robot end-effector material
• Fan Filter Unit speed/balance	• Humidity
• Exhaust Flow Rate	• Temperature

- Issues associated with using product wafers/scans required development of alternative evaluation methods
  - An electrical discharge mechanism suggested surface charge evaluation techniques could be informative

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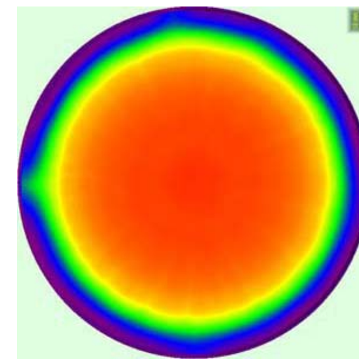
ChemetriQ® Charge Measurement

- Fab25 worked collaboratively with Qcept Technologies and SEZ to investigate arcing phenomenon using ChemetriQ metrology
- Tool has advantages over existing Fab25 surface charge metrology capability including
- Charge Inspection

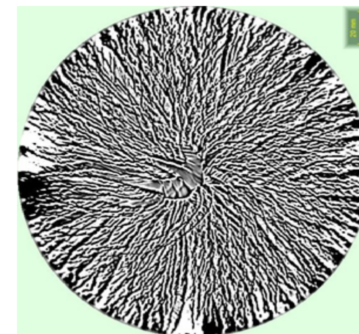
  Speed - 6 minutes/wafer scan @ 200mm

  Resolution- ~3 million points/wafer @ 200mm

ACM (charge) Image



NVD Image



- Non-Visual Defects (NVD) Inspection
  - Detect Sub-monolayer Non-Visual Residues
  - Organics, Inorganics, Metallics, Watermark
- Charge + NVD Inspection
  - Complete Characterization for Wet Clean Processes

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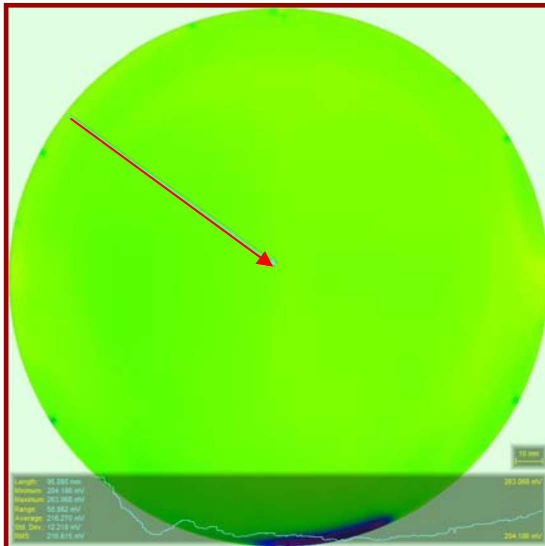
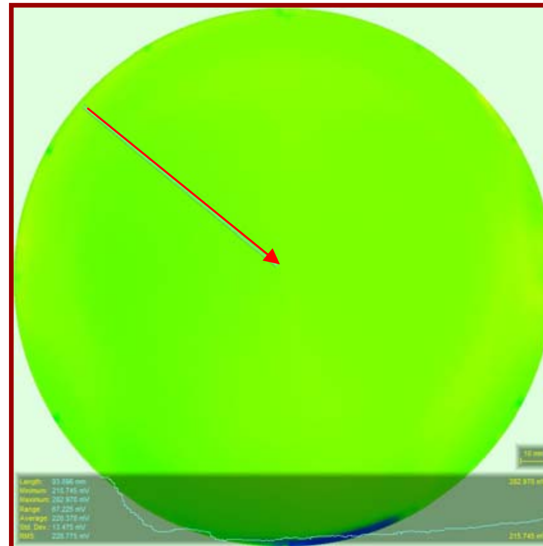
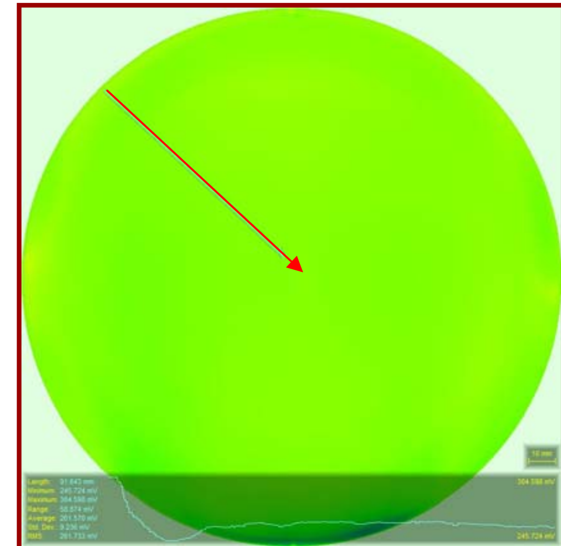
Qcept Surface Charge Study – Wafer Handling

Ion Bars Off, handling only	Ion Bar Opt, handling only	Bare TW no processing
		
Line graph min = 0.20 V, max 0.26 V **Range 0.06 V**	Line graph min = 0.21 V, max 0.28 V **Range 0.07 V**	Line graph min = 0.25 V, max 0.30 V **Range = 0.05 V**

- Wafer Handling does not appreciably impact surface charge on wafers
- Wafer charging during handling is not affected by Ion bar functionality

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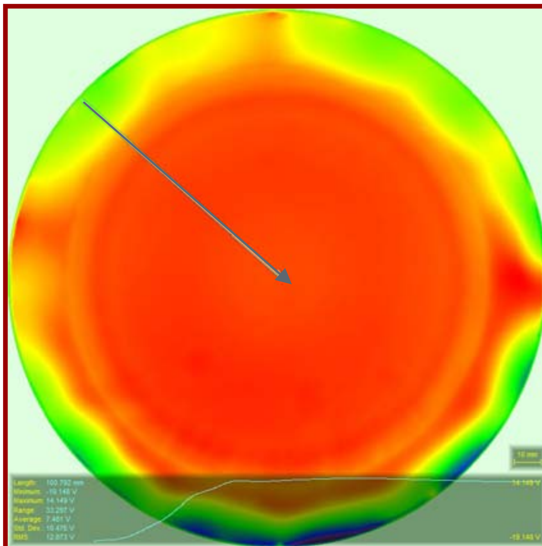
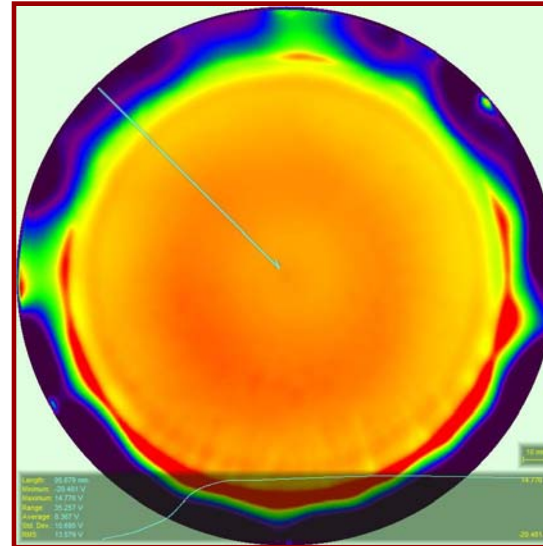
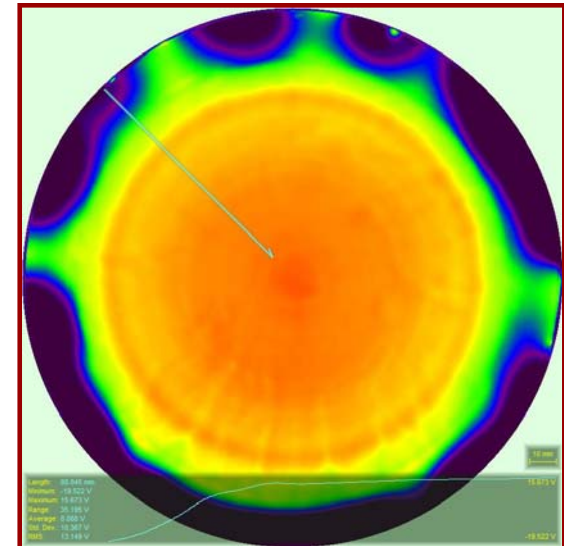
Qcept Surface Charge Study
Ion Bar Setting Impact on W/S Process

Ion Bars Off, full process	Ion Bars Opt, full process	STD Full Process
		
min = -5.5 V max 3.1 V **Range = 8.6 V**	**min = -5.0 V max 3.7 V** **Range 8.7 V**	**min = -4.8 V max 4.1 V** **Range = 8.9 V**

- Wafer Maps demonstrate significant wafer surface charging differences from 'handling only' wafers
- Minor differences in range and absolute voltage detected wrt Ion Bars

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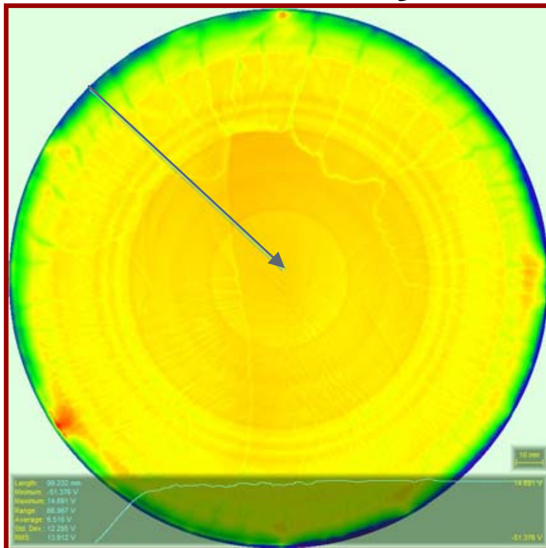
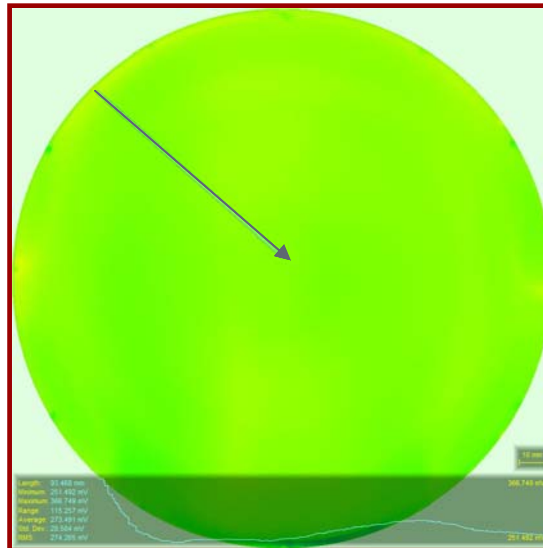
Qcept Surface Charge Study – DI Rinse/N2 Dry

DI/N2 only



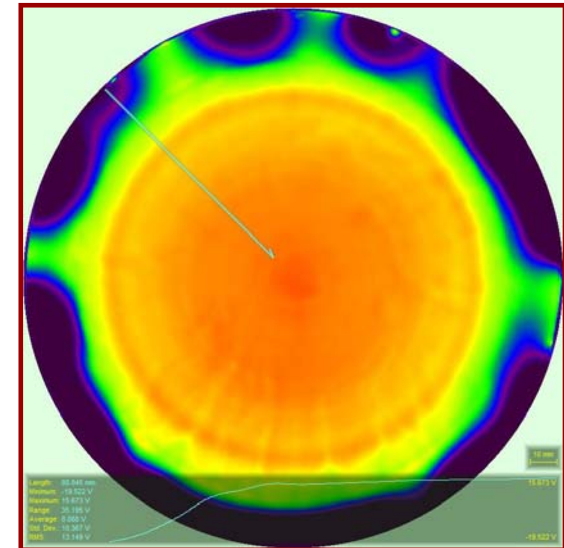
min = -11.2 V max 3.0 V
Range 14.2 V

N2 Dry only



min = 0.25 V, max 0.37 V
Range = 0.12 V

STD Full Process



min = -4.8 V max 4.1 V
Range = 8.9 V

- Wafer Maps demonstrate significant wafer surface charging associated with DI rinse step

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Qcept Surface Charge Study
Impact of Spin Speed on Surface Charging

Reference Wafer No Process	Full Process: Low Spin Speed	Full Process: STD Spin Speed	Full Process: Hi Spin Speed	DI/N2 Only
	Range –27V	Range –37V	Range –350V Saturated	Range –165V

- **Wafer Surface charge substantially impacted by spin speed**
- **Suggests charging mechanism is due to friction between DI Rinse water and wafer surface**

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How to Reduce Charging in DI Rinse Step

- **Surface charge data suggests arcing mechanism is driven by interaction of high purity DI water and wafer surface**
  - **High resistivity water (18 MOhm) delivered to wafer surface results in generation of free electrons that cannot recombine within the water stream**
  - **Electrons build on oxide surface during rinse step until dielectric threshold is exceeded and charge differential is resolved via an arc**
- **If this mechanism is correct, adding charge carrying capacity to DI rinse will prevent arcing**
- **Collaboration with SEZ America led to proposal to evaluate impact of adding CO2 to DI rinse on surface charge**

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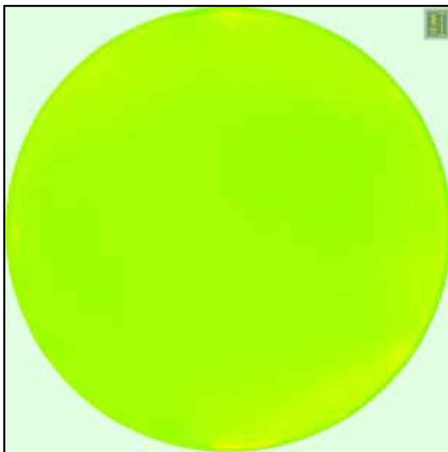
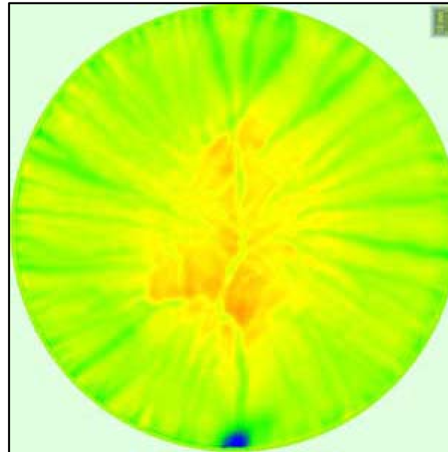
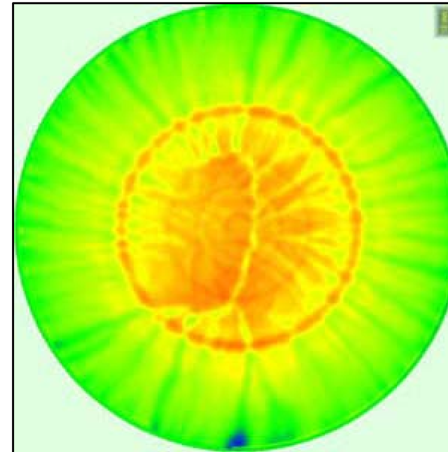
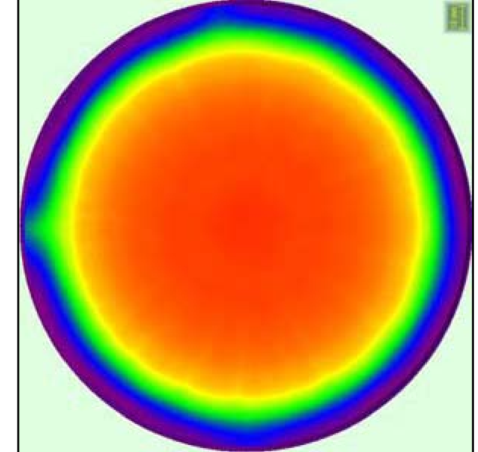
Impact of DICO2 on Surface Charging

Reference Wafer No Process	Full Process DI rinse w 30 kOhm	Full Process DI rinse w 150 kOhm	Full Process DI rinse w/o CO2
			
	Range ~1.1V	Range ~2.3V	Range ~37.0V

- **Addition of CO2 to DI rinse Water (30k Ohm) significantly reduces surface charging phenomenon**

- **Is BEOL/Product integration compatible with use of DICO2?**

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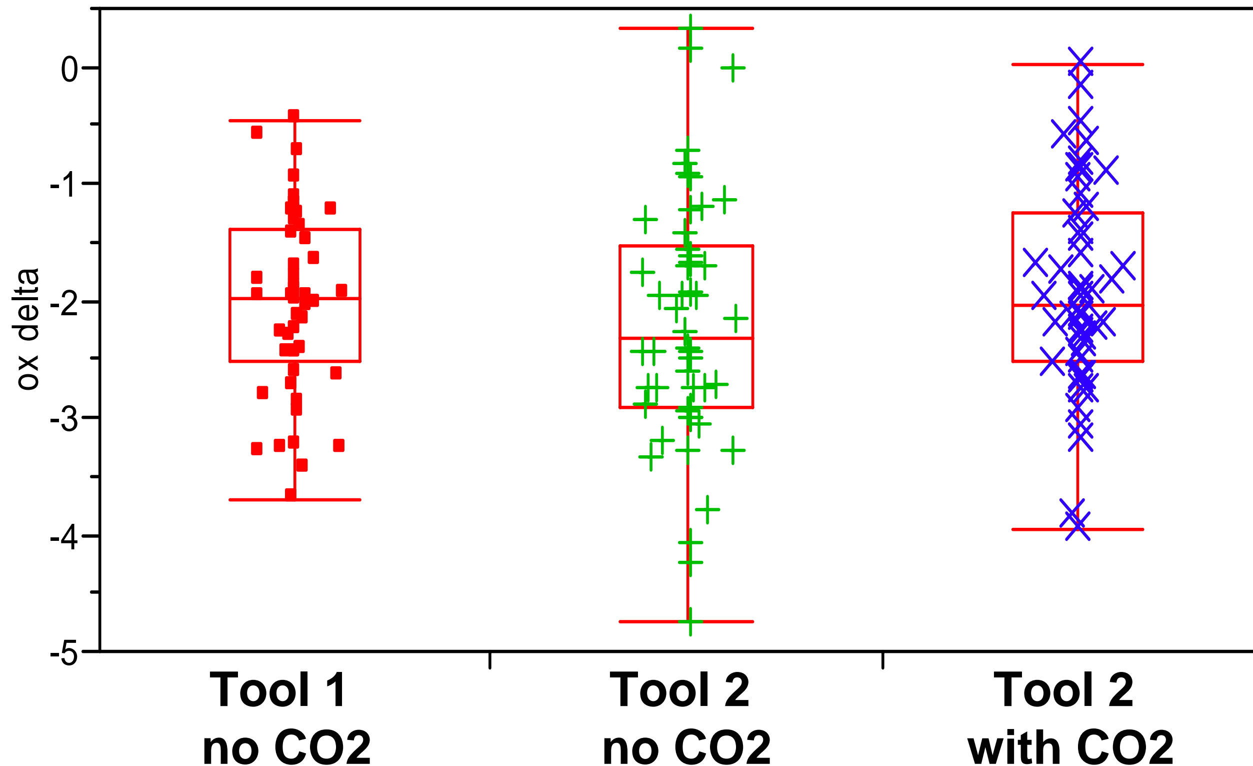
DICO2 Impact on Oxide Removal (Optiprobe)



- Substrate 1K Thermal oxide, 180 sec DICO2 exposure @ 30kOhm resistivity
- No difference in Oxide removal observed
- No impact on n or k values (data not shown)

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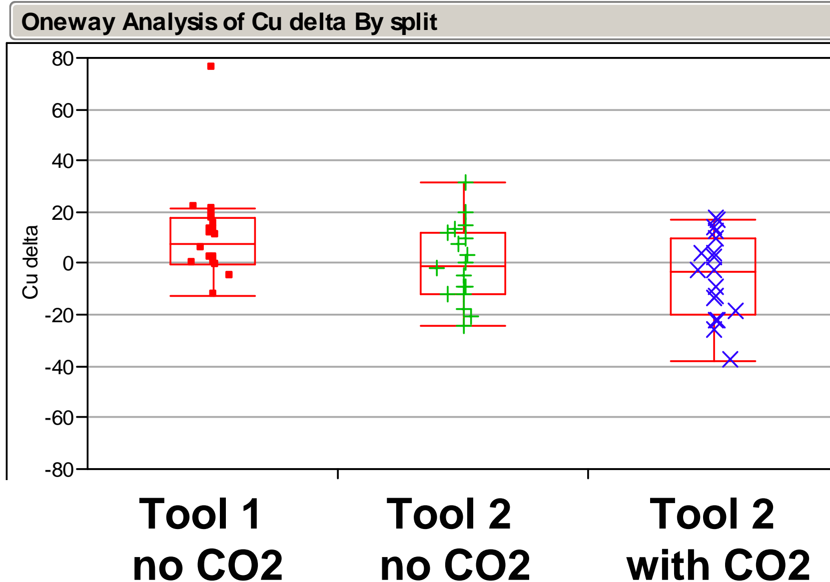
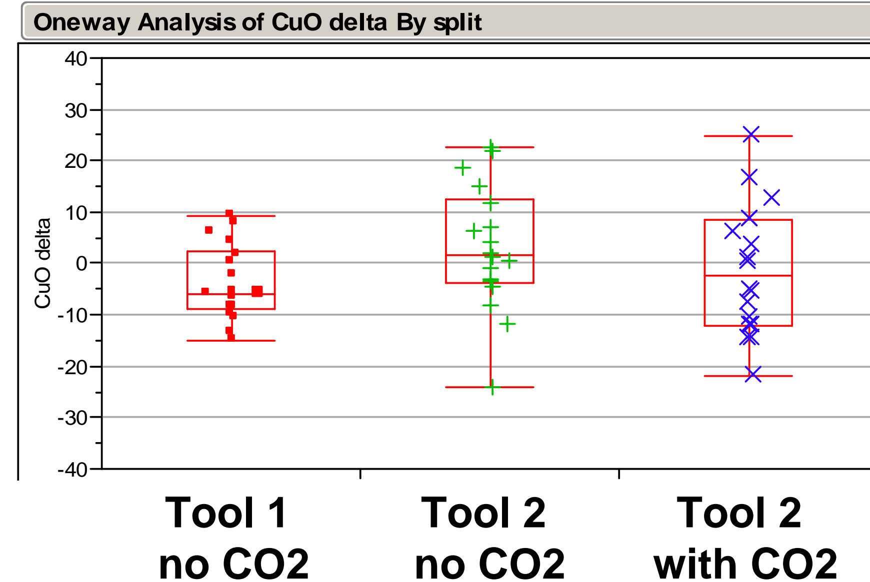
DICO2 Impact on Cu and CuO (XRR)





Tool 1 no CO2 | Tool 2 no CO2 | Tool 2 with CO2

Tool 1 no CO2 | Tool 2 no CO2 | Tool 2 with CO2

Substrate: Cu 'seed' wafers, ~ 600Å Cu

No significant difference in Cu or CuO removal

Increased variation/range observed from wafers run on SEZ platform 2

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DICO2 Impact on Cu Rs (4 point Probe)

Rs delta = post - pre

Delta Rs

20
10
0
-10
-20

Cu Seed Tool 1 no CO2	Cu Seed Tool 2 no CO2	Cu Seed Tool 2 with CO2	Polished Tool 1 no CO2	Polished Tool 2 no CO2	Polished Tool 2 with CO2

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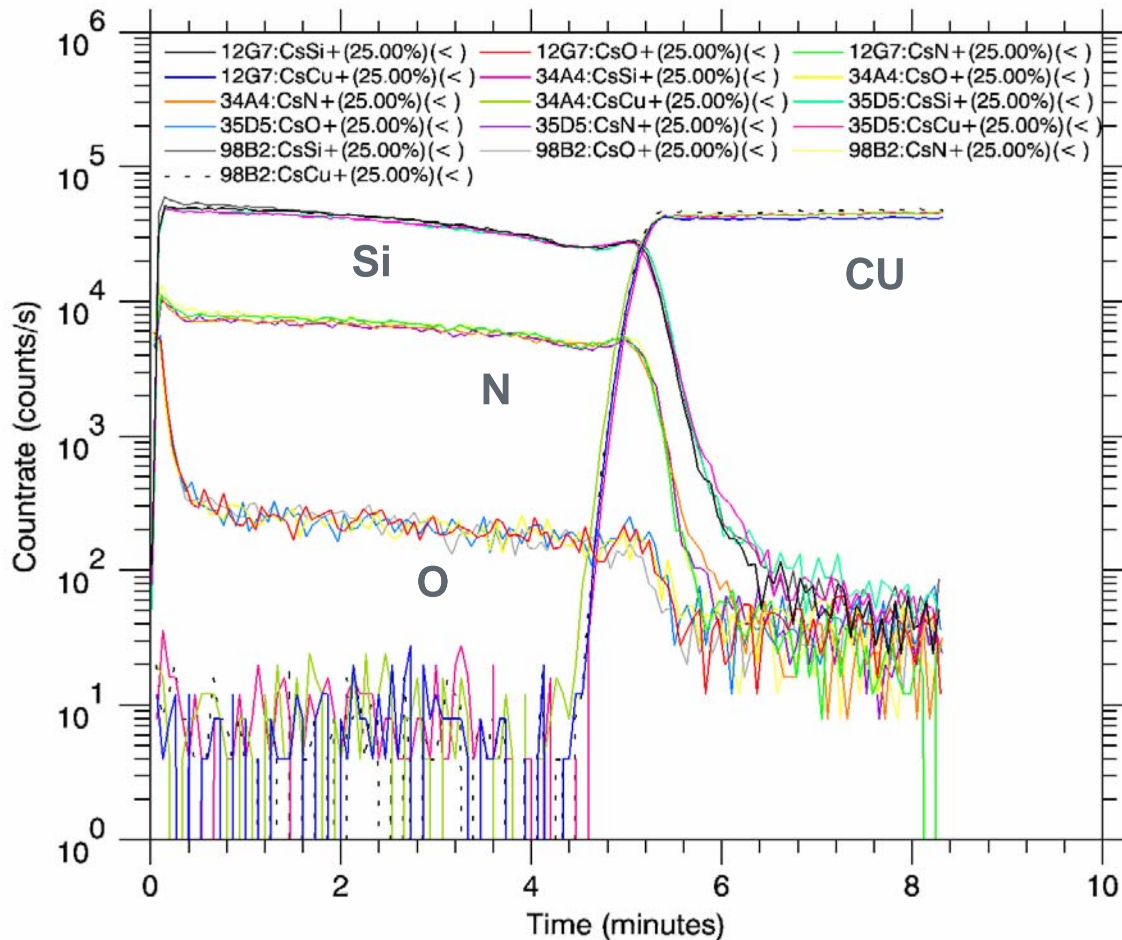
Quad SIMS Data (Overlay Plot)



Substrate

Wafer	Condition
98B2	Control
35D5	SEZ plat. 1 no CO2
12G7	SEZ Plat. 2 no CO2
34A4	SEZ plat. 2 With CO2

No significant differences in profile noted

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Additional Product Testing

Wafer Electrical Test (WET)	WET data analysis of 'split' lots and volume trial indistinguishable from non-CO2 material
Sort (Yield)	SORT yield improved for CO2 processed material
Wafer Level Reliability (WLR)	No significant shifts from baseline with DICO2 processed material
Wafer Level Voltage Regulated Dielectric Breakdown (WL-VRDB)	No significant shifts from baseline with DICO2 processed material for interfaces tested
Electro Migration	No significant shifts from baseline with DICO2 processed material for interfaces tested
Stress Migration	No significant shifts from baseline with DICO2 processed material for interfaces tested

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DICO2 Impact on Detected Arcs

Month	Etcher Arcs	SEZ Arcs No CO2	SEZ Arcs with CO2

Arc defect frequency falls as % of wafers run with CO2 increases

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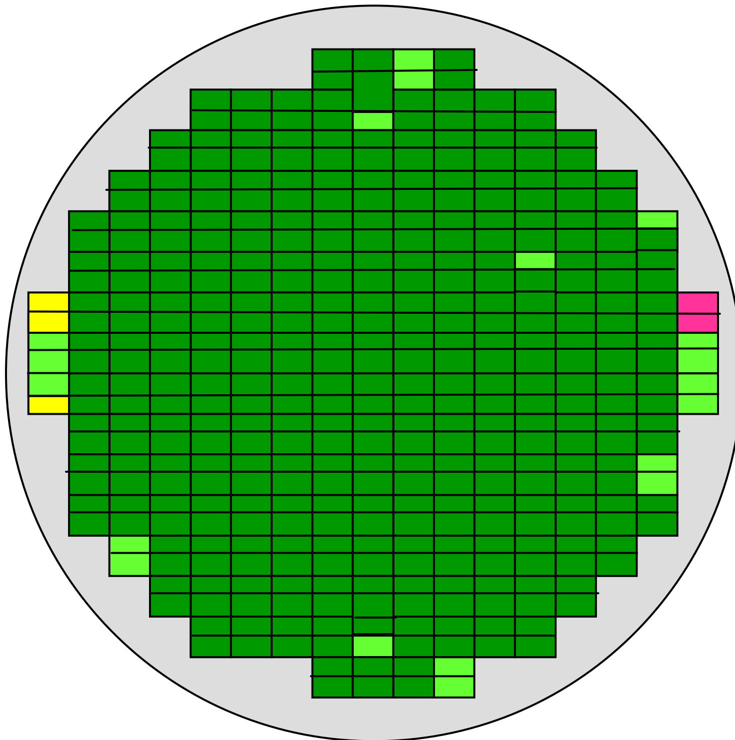
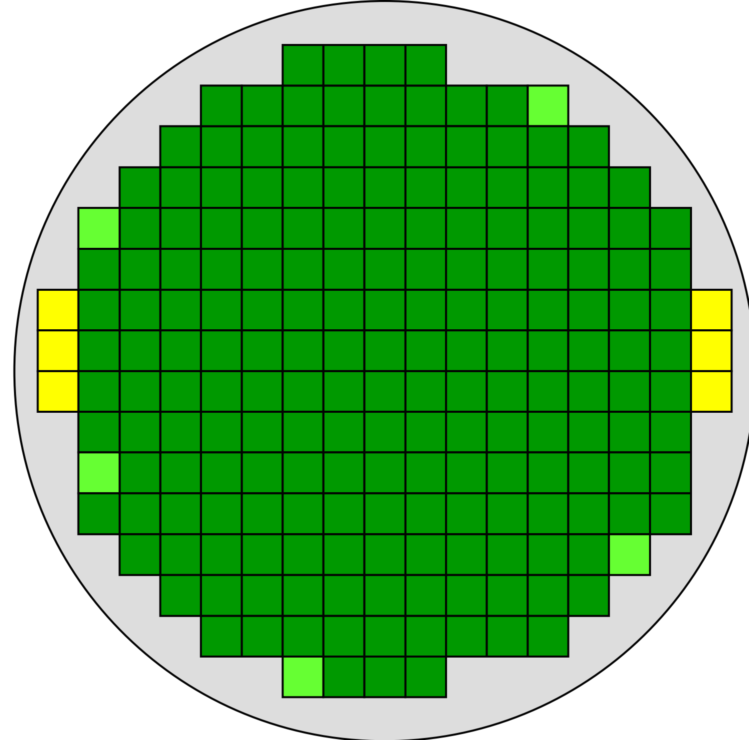
Relative Yield Analysis Post CO2 Implementation – Composite Wafer Maps

Product X



Product Y



- **Stacked wafer maps (~120 wafers) center donut region with reduced yield has been eliminated on wafers run with DICO2**

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Conclusions

- Single wafer Spin Processing with high resisitivity DI rinse steps can lead to arcing with significant impact on yield
- Reducing DI resistivity by addition of CO2 reduced arc formation and eliminated donut pattern of reduced yield
- Addition of CO2 has no known negative impact on any product or test wafer substrates
- Collaborative approach between Spansion, Qcept, and SEZ allowed comparatively rapid learning and implementation of a solution to improve yield

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Appendix

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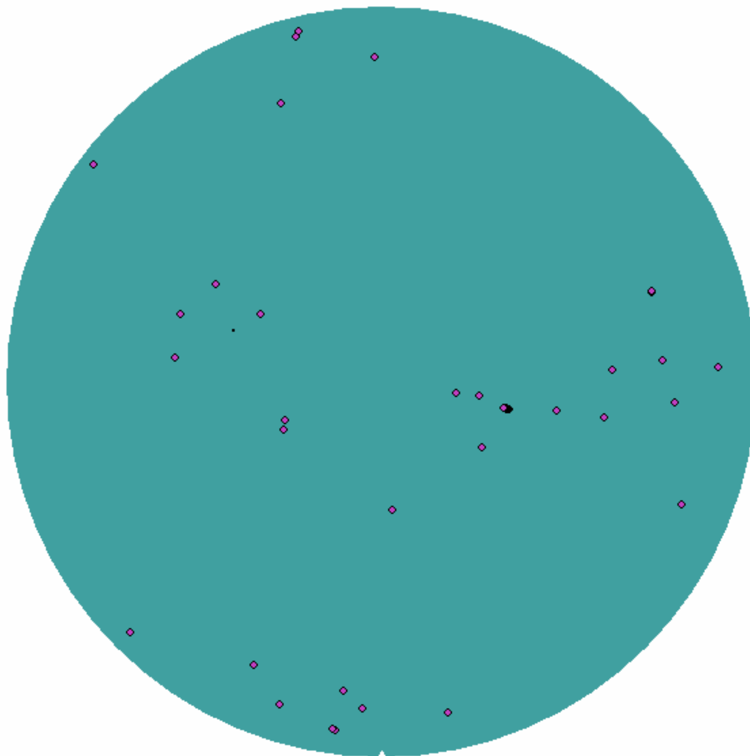
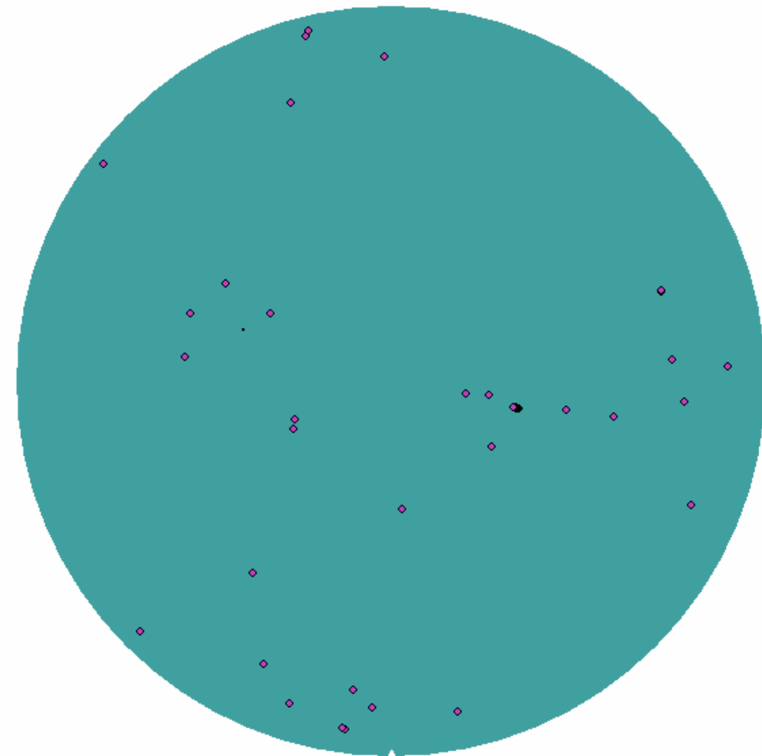
SP1 Defect Scan Pre/Post DICO2 Exposure

Cu 'Seed' wafer Pre-Scan



Post-Scan after 180 sec DICO2 (30K Ohm)



Extended DICO2 treatment has no Impact on bare Cu wafer defectivity

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