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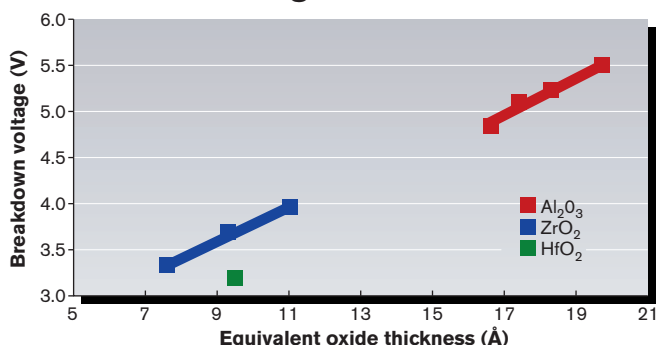
Components
and Subsystems
Supplement



Charge Mapping for
High-k Integration

Controlling Process-Induced Heightens Productivity

Breakdown Voltage vs. Oxide Thickness

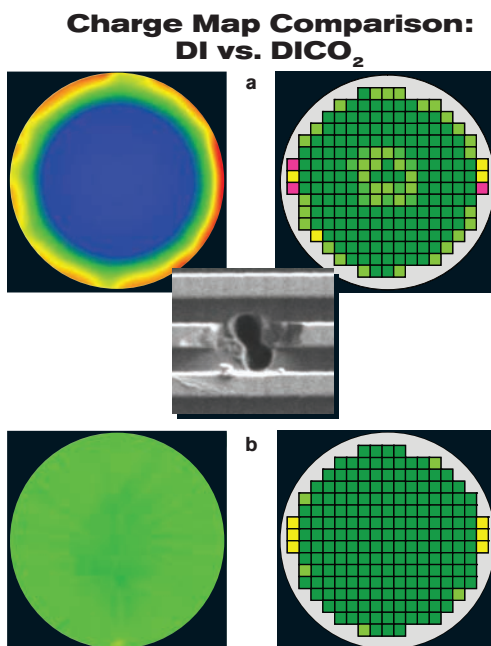


1. Breakdown voltages for various high-k gate dielectrics as a function of EOT. Single-wafer cleans processes can easily generate voltages well above these levels.

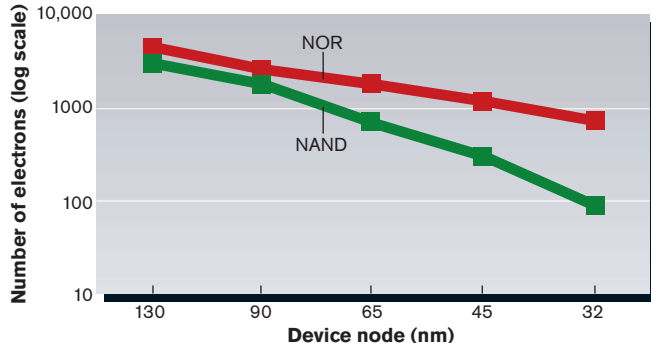
As new materials and processes are introduced into 45 nm devices, process-induced charge effects present a serious and growing yield-critical issue that requires a renewed focus on minimizing and controlling charge during wafer processing. Unlike the stable materials used in past generations, less robust low-k dielectrics, high-k/metal gate films, advanced copper metallization schemes, plasma-enhanced film deposition, and thinner metal barrier layers are all subject to yield-limiting charge issues.

The defect category known as non-visual defects (NVDs) includes process-induced charging as well as organic and metallic residues. NVDs can impact device performance in three ways: physically causing electrostatic discharge events and galvanic metal corrosion, electrically resulting in shifts in critical device performance characteristics, and in-field reliability leading to changes in critical parameters such as time-dependent dielectric breakdown. Charging can occur during both wet cleans and plasma-based processes such as etching, ashing and dielectric film deposition. Of particular interest is the introduction of single-wafer cleans, which has been shown to induce significant charge levels that can directly result in yield loss.

3. A 37 V charge gradient corresponding to yield loss regions (a) due to electrostatically induced “explosions” that damaged metal runners (inset) and a reduction in the gradient to ~2 V following the introduction of CO₂ to the single-wafer rinse DI water (b).



Stored Electrons vs. Device Node



2. The number of electrons stored per bit of flash memory is plunging, making these devices more susceptible to damage from process-induced charge.

This article describes the sources and yield impact of process-induced charge defects, how they relate to the integration of new materials and processes, and the need to incorporate charge detection as part of a comprehensive yield management strategy.

Generating NVDs

The levels of charging that had little to no effect at previous design rules can now damage structures through electrostatic discharge events and shift critical device performance characteristics through charge trapping. The impact is heightened as gate structures migrate to lower operating voltages and tighter process windows for parametric control.

New integration schemes comprising complex device structures, new processing techniques and materials are less tolerant to contamination and therefore require cleaning techniques that could increase the incidence of process-induced charging and NVDs. For example, as aspect ratios for deep trenches and the complexity of vertical gate structures continue to increase, the industry is migrating to single-wafer cleans tools, which use a combination of physical and chemical forces to remove residue from wafers. In particular, high-velocity sprays that can lead to process-induced charging are increasingly used to clean these structures.

Cleaning requirements are heightened for many new materials as well. It is increasingly understood that the electrical properties of high-k and low-k dielectrics

Charging

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Process-induced charge defects are becoming a yield issue for next-generation devices, prompting the need for enhanced control during wafer processing.

can be severely compromised by high temperatures, leading to an increased reliance on lower-temperature processes such as anneal steps. However, this in turn increases the risk of organic residue contamination, as organics that may have volatilized at higher temperatures are now left on the wafer surface at lower temperatures, and must be removed. And more backside and edge cleans are being introduced into production as new materials pose new concerns about cross-contamination¹ from shared equipment and carriers.

Another driver for edge cleans is immersion lithography. A critical side effect of this technique is that any contamination present on the edges of wafers, whether metallic or organic, can be transferred to the interior of the wafer during the imaging process. This, combined with the variety of new materials being introduced into the line, is leading to an increased focus on defect-free wafer edges, and again, the need for edge cleans.

Impact of new materials

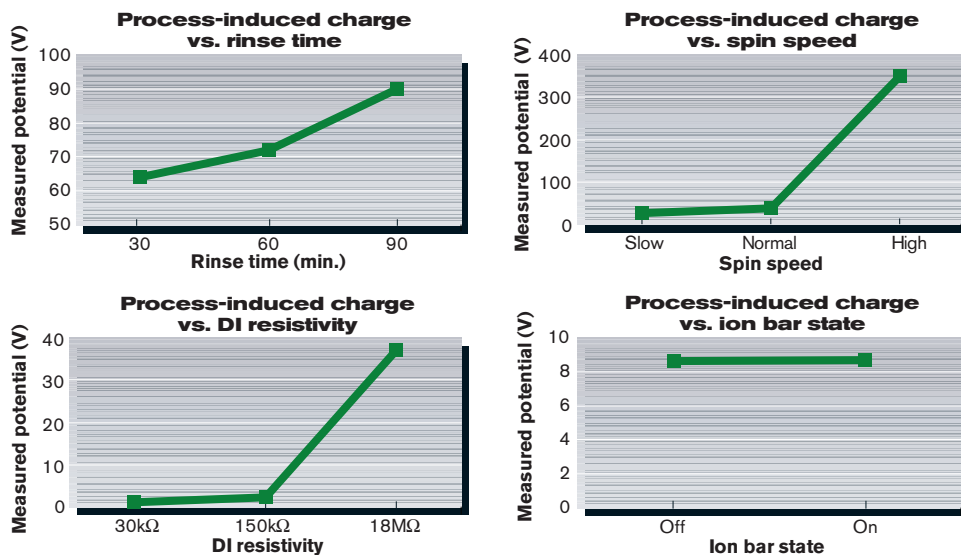
The increased reliance on single-wafer cleans and the introduction of new, more fragile materials are enough to make process-induced charging control a particular point of interest. The num-

bers speak for themselves. For example, while silicon dioxide (SiO_2) has a published breakdown voltage (V_B) of 10 MV/cm, figures for hafnium dioxide (HfO_2) are a factor of 6 smaller, at only 1.8 MV/cm. The implication is that charge-induced yield loss for high-k devices can occur at significantly lower voltages than for conventional devices at a given physical dielectric thickness.

The problem is made even more challenging by the wide variability in actual breakdown voltages, depending on the processes used. The inclusion of carbon into an SiO_2 structure, for instance, can reduce its V_B by as much as 5x. When V_B for various high-k dielectrics expected for advanced gate stacks is plotted against equivalent oxide thickness (EOT) (Fig. 1)², it becomes clear that since single-wafer cleaning tools induce voltages significantly above these levels, there is risk of damage to devices.



Impact of Cleaning Parameters on Wafer Charging



4. Test results indicate that spin speed, rinse time and DI resistivity have significant influences on charging the wafer, whereas ion bars have little effect.

shown in the stacked die yield map, the highest charged areas — both positive and negative — correspond to areas of lost die yield.

The addition of CO₂ to DI water solved this problem by significantly increasing its conductivity due to the formation of carbonic acid, and reduced wafer charging during the rinse cycle. A reduction in potential to the 1.2 V range, with corresponding improvement in yield for both the center and edge die regions, was demonstrated (Fig. 3b).

Through further inspection of single-wafer cleaning, there is a correlation between the magnitude of the induced

potential to rinse time, spin speed and DI resistivity. However, the magnitude is not affected by the use of ion bars, a popular option on clean tools, during processing. The spin speed and rinse times were varied around the nominal process conditions, using 18 MΩ DI water (Fig. 4). As shown, the detected surface voltage range increases significantly with spin speed — as high as 350 V, easily high enough to cause serious yield and/or reliability problems on device wafers. Even with the lowest spin speed, there was sufficient surface potential to cause yield loss. Rinse time is also shown to correlate with charging levels in an approximately linear fashion. The use of ion bars appears to have little effect on controlling charging, implying that the charging is persistent once introduced to the wafer surface.

Thus, the choices made in materials integration can have a dramatic effect on a device's critical level of charging. Another way of looking at the problem is to compare process-induced charge with the charge necessary to store a bit in floating memory-based flash devices (Fig. 2).³ This value will plunge over time: for NAND, from 700 electrons per bit at the 65 nm node to 90 electrons per bit for 32 nm. Adjusting for cell XY scaling, this means a decrease of ~40% in area charge density over time, making both the storage structures and the associated sense circuitry that much more susceptible to damage. However, this can be remedied if process-induced charge is reduced or design margins are increased (with an associated impact on performance).

Outright failures that occur during processing are just one possibility. Even sub-breakdown levels of trapped charge may be detrimental to device performance. The presence of fixed charge in HfO₂ gate dielectrics, for example, may impact work function extraction, mobility and reliability, and these effects can be expected to be significant.⁴ Furthermore, incomplete removal of indium antimony oxide (InSbO₂) has been shown to result in charge traps that degrade the performance of InSb-based devices.⁵

Charge defects in single-wafer cleans

Rinsing with 18 MΩ deionized (DI) water has long been associated with a negative surface potential on wafers. However, the charge profiles are far from uniform. In fact, there are often regions on the same wafer that are oppositely charged. Based on internal studies, there is generally a negative charge buildup at the center of wafers, as expected, but also a strong positive charge ring around the outside of wafers that also causes yield loss. Others have reported identifying a yield loss mechanism caused by charge buildup during DI water rinsing, which produced opens and shorts in metal runners.⁶

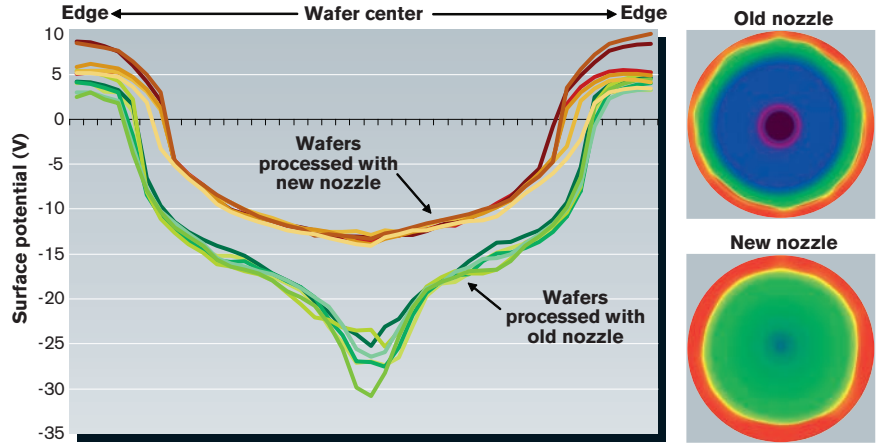
Investigating how much voltage can be induced by a single-wafer clean, a ChemetriQ® charge mapping was performed on a 1000 Å thermal oxide, showing a 37 V range of potential built up across the wafer from edge to center (Fig. 3a). The blue region at the center of the wafer represents areas of negative charging, and red areas on the outside of the wafer represent positive charging. As

Although it is a relatively simple matter to reduce the magnitude of charging by the introduction of CO₂ to the DI, this does not come without cost and it adds a further complication to the rinse optimization. The addition of CO₂ lowers the pH of the water from neutral to as low as 5.0, which is associated with carbonic acid formation. The introduction of 20 kΩ DICO₂ to DI has been reported to increase the incidence of corrosion on copper lines, forcing two different CO₂ concentrations to be used at two different processing steps,⁷ while another report discussed how there is still sufficient charging to induce “explosions” in films even when DICO₂ is used.⁸

However, it is still important that charge be controlled before it is introduced onto the wafer surface, because the induced charge may be very persistent — even in the presence of ionizers, as our experiments have confirmed. In one experiment, for example, the charge profile of a CVD oxide wafer was measured over time. Beginning in a charged state of ~5 V, the charge level remained stable, falling only when the wafer was directly exposed to an ionizer. However, even then, the decrease was at a rate of ~2 V per hour of ionizer exposure. This suggests that the few seconds a wafer is exposed to an ionizer bar in a typical process tool is not an effective means of managing the charging problem — charge control is necessary before the charge is introduced to the wafers as it may readily persist onto the next processing step.

The mechanical configuration of the rinse equipment can also have a significant impact on charging. Figure 5 shows a compari-

Influence of Nozzles on Induced Charge



5. A new rinse nozzle configuration reduced peak charging at the center of the wafer by approximately half, but doubled the charging around the wafer edge.

son of two sets of wafers, using two configurations of nozzles. We converted the charge maps to radial profiles to more easily make comparisons among the groups of wafers. These profiles show that the old nozzle produced potentials in the 25-30 V range, and the new nozzle reduced the range of potentials by more than a factor of 2 to 12 V. However, the new nozzle also produced more charging at the wafer edge, in the 5-8 V range vs. 2-4 V with the old nozzles.

Alternate wafer cleaning technologies that use low-conductivity liquids, solids or gases (e.g., supercritical fluids, solid CO₂, argon “snow,” etc.) may also generate significant charge buildup on wafers, leading to yield loss and/or insufficient device reliability. Before these alternate wafer-cleaning technologies can be used in high-volume IC manufacturing, their ability to induce charging on wafers must be studied. In addition to the control of final rinse conductivity, wafer charge buildup can be affected by the pH of the post-etch stripper,⁹ and airborne molecular contaminants (AMCs) in the environment.

Process-induced charge

Plasma processing (etching, ashing and plasma-enhanced dielectric film deposition) typically produces a positive surface potential on wafers, with different gradient profiles than those typically seen on wet wafers. Ion implant tools contain systems to neutralize surface charge, but when they are not optimized, or malfunction, implanting can produce either a positive or negative wafer surface potential.

For example, one fab was seeing degradation of electrical device characteristics in the upper right quadrant of wafers processed on a particular etcher, with no apparent cause that could be identified using optical defect inspectors. The ChemetriQ maps clearly showed that the “poor” tool-induced charge gradients of -4 V that the “good” tool did not, which correlated to the variation of the critical electrical characteristic. Interestingly, the “good” tool did show consistent positive charging in the 2-3 V range, but without a gradient.

Other examples of etch-related charge issues have been published. An electrogalvanic corrosion process for tungsten plugs driven by positive charge buildup on patterned wafers during metal etching was identified.⁹ Another group reported etch process-induced electrogalvanic corrosion of titanium barrier layers near unlanded vias.¹⁰ Further, it has been demonstrated that charging of wafers during O₂ ashing can lead to a “punch-through” type of defect where opens occur due to missing copper.⁷

In yield management and new materials integration, it is critical that a high percentage of “good” devices is maintained while minimizing processing times. In order to quickly ramp and maintain yield, yield management must incorporate inspection solutions that can detect process-induced charge issues to:

- Optimize yield learning during development and ramp.
- Monitor the production line for charge-related excursions.

These needs call for fast, full-wafer inspection that can easily be tied into existing yield management systems, as is done today for physical defectivity such as particles. Such an inspection solution must be able to:

- Inspect full wafers at production-worthy speeds.
- Inspect patterned and blanket wafers.
- Output trendable metrics for SPC purposes.
- Interface to the fab using standard interfaces and file formats.

As seen in earlier examples, full-wafer inspection is required to understand and properly capture process-induced charge defects, as the nature of the charging is non-uniform across the wafer surface. Random point measurements are not sufficient to capture the full range and spatial distribution of charging as seen on these wafers.

Conclusions

While yield management — development, ramp and full production — has traditionally focused on optical inspection to drive yield, NVDs cannot be detected by traditional optical inspection because they do not scatter light and thus are not detectable optically. Other means by which such charge can be detected either measure only point defects (such as Kelvin probes) or are destructive in nature, and thus are not sufficient to address this growing problem.

A new technology has been developed and is currently available, called Qcept™ Surface Potential Difference Imaging (SPDI), which allows the capture of NVDs. As shown in Figure 6, SPDI uses a metallic probe, placed close to a moving wafer surface, to detect changes in surface potential, which are directly affected by NVDs. In this system, as the wafer is rotated, areas of non-uniformity are passed under the probe. The probe detects the voltage potential changes associated with these non-uniformities, which are captured by the system and assembled into an image. In this way, the entire surface of the wafer is measured, ensuring that all regions of charging are accurately captured, including the bevel region.

After the image has been captured, it can be processed to extract the relevant SPC metrics for the process — in this case, the charge range of the wafer. These metrics can be uploaded to the fab host or sent to yield management software systems via standard file formats to allow for real-time control of the process. In this way, excursions caused by such issues as improper DI conductivity in wet clean tools, chuck/de-chuck issues in plasma tools, or plasma flood charge malfunction in implant tools can be detected and corrected before they have a chance to impact yield.

The challenges of integrating new materials and processes demands a more comprehensive yield management strategy driven in

Controlling Process-Induced Charging

part by a growing sensitivity to yield-limiting, process-induced charge issues. The availability of new technologies such as SPDI may answer the need for enhanced detection and control of NVDs.

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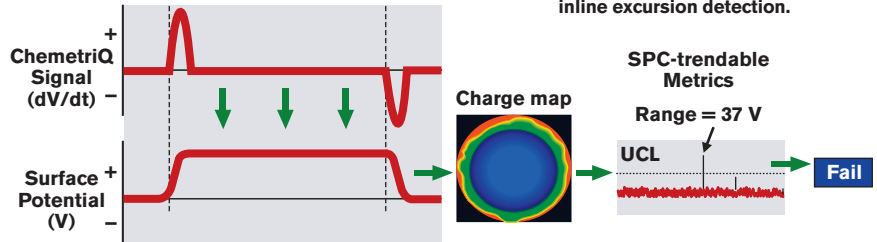
Surface Potential Difference Imaging



6. An SPDI system detects the surface potential non-uniformities associated with process-induced charging defects, producing SPC-based metrics that can be used for inline excursion detection.

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