Non-visual defect inspection for comprehensive yield management

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As new materials, processes, and structures are introduced at sub45nm nodes, surface quality requirements are becoming more stringent. Surface quality control issues can give rise to organic and metallic residues, charging, and other non-visual defects (NVDs). Whereas yield management strategies previously focused solely on physical defects such as particles and scratches, NVD inspection is becoming an integral part of yield management at these nodes.

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NVDs are defects that do not have measurable physical dimensions in the traditional sense. While they can cover large areas of a wafer's surface, they are often sub-monolayer or electrical in nature, having the Z-height of a single atom or molecule. NVDs cause changes to the electrical or chemical properties of the wafer surface that can lead to poor adhesion of subsequent layers, degraded device parametrics or long-term reliability issues. The International Technology Roadmap for Semiconductors (ITRS) cites the increasing importance of NVDs for yield, and the need for new NVD inspection techniques at advanced design nodes [1].

Many NVDs result from suboptimal cleaning and surface preparation due to the liquid-contact nature of the step. These NVDs can come from the wafer, the liquid, the interaction between liquid and wafer, or the environment. NVDs include:

- **Organic contamination.** For example, new resist formulations or etch processes may result in incomplete resist stripping when cleaned using an existing process of record.
- **Metallic contamination.** For example, copper (Cu) contamination of a bath can cause subsequent cross-contamination of wafers exposed to that bath.
- **Process-induced charge.** Charge can buildup on the wafer's surface during the final rinse, especially on insulators cleaned in single-wafer tools.
- **Carrier-induced outgassing.** Plastic containers such as FOUPs and FOSBs can outgas compounds that react with residual wafer cleaning solvents to form insoluble organic salts at locations close to the carrier touch points.
- **Airborne/surface molecular contamination.** Adsorption of AMCs during wafer queuing can lead to surface molecular contamination, which may be the AMC

species or a compound formed by the AMC species and the material on the wafer surface.

NVD defect detection is quite different than for physical defects, such as particles. Because of their relatively large height, physical defects scatter incident light. They are typically detected using optical inspection techniques, such as brightfield and darkfield imaging or laser scatterometry. NVD Z-height is too small to scatter light, precluding optical detection.

I review a new NVD inspection technique, describing several case studies of NVD issues impacting yield, and explore the economics of NVD inspection.

Incorporating NVD inspection into yield management

Because optical inspection techniques cannot detect NVDs, other means are needed. One such technology is the ChemetriQ system, which uses surface potential difference imaging (SPDI) to detect changes in the work function and charge of materials [2].

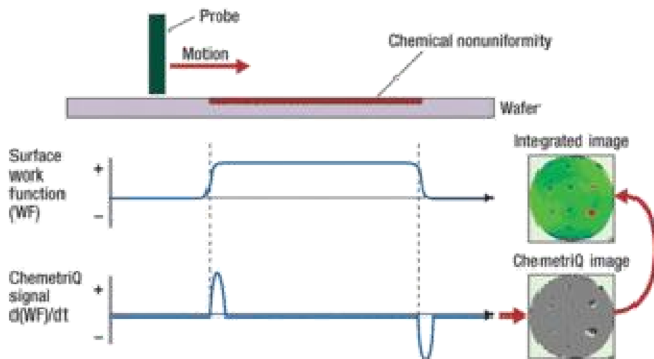

Figure 1. *The SPDI method uses work function sensing to detect NVDs on the wafer surface.*
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The SPDI method spins the wafer and holds a probe close to (but not contacting) the wafer surface (Fig. 1). Where the surface is completely uniform, a constant voltage results that is proportional to the difference in work functions of the probe and the wafer. When a non-uniformity is encountered, the change in work function causes a change in voltage on the probe tip, which is proportional to the rate of change in work function on the wafer, d(WF)/dt. This change is detected and mapped over the entire surface of the wafer to form the ChemetriQ image in Fig.1. A simple mathematical integration then produces the integrated image that shows regions of NVDs on the wafer.

With the increasing impact NVDs have on device yield, yield management strategies must incorporate NVD inspection and review in a way that is analogous to physical defect inspection ? both in-line to prevent excursions that can affect line yield, and in the lab to assist with root cause analysis and process development. Inspection can help pinpoint NVDs in production. These locations can then be exported to analytical tools such as TXRF or TOF-SIMS, which provide detailed summaries of NVD materials.

In the following examples of NVDs impacting device yields, practical implementation of NVD inspection isolated their source and eliminated the NVDs.

Process-induced charging in a 45nm logic fab

Process-induced charging is a growing source of yield loss. New materials, thinner film stacks, and smaller geometries are more easily damaged by charge. New techniques such as single wafer cleaning can introduce new sources of process-induced charge into the process. Because charging cannot be detected by optical inspection, traditional yield management tools are "blind" to this issue.

A major logic manufacturer recently experienced a charge-related yield issue on its 45nm line [3]. End-of-line yield maps (Fig. 2a) showed that center dice covering ~2% of the wafer were consistently non-yielding. Further analysis via tool commonality studies pinpointed the probable source to a specific chamber on a single wafer cleans tool. However, none of the existing inspectors in the production line were able to capture a defect pattern matching this center of wafer signature, making it impossible to isolate the source and eliminate the root cause of the yield loss.

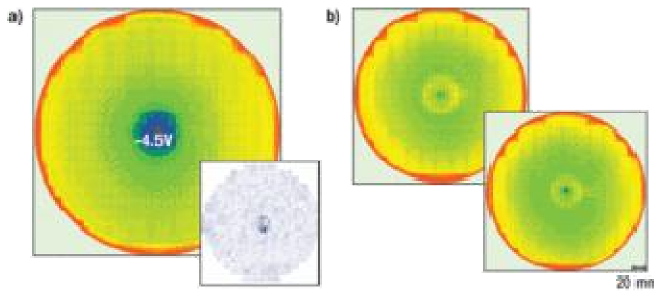

Figure 2. *End-of-line yield maps correlated to a charging signature from a single wafer clean tool a) that was significantly different from other tools b).*
Click here to enlarge image

SPDI inspection, however, highlighted a center of wafer charge gradient, whereby the outer regions of the wafer exhibited a -1.5V charge level compared to -4.5V for the center area. Comparisons were done to other chambers running the same cleans process, which showed much lower levels of center-of-wafer charge (Fig. 2b). The process engineers designed and performed a number of experimental splits to better understand the nature of the charge signatures, and to assess how tool and process parameters contributed. The experimental results indicated that the charge levels could be optimized with a tool configuration using a shield plate, N_2 ambient purge, and a 60sec. dilute HF etch time.

Organic contamination in a 32nm DRAM fab

Innovative resist formulations are in development for advanced design rules. In the front end, more complex structures, double-patterning, and immersion lithography are driving these new formulations. In the back end, new integration and interconnect schemes also

encourage new lithographic techniques with new resist requirements. A critical issue in using new resists is that if they are not completely stripped from the surface after etch, organic NVDs can cause subsequent adhesion and reliability issues.

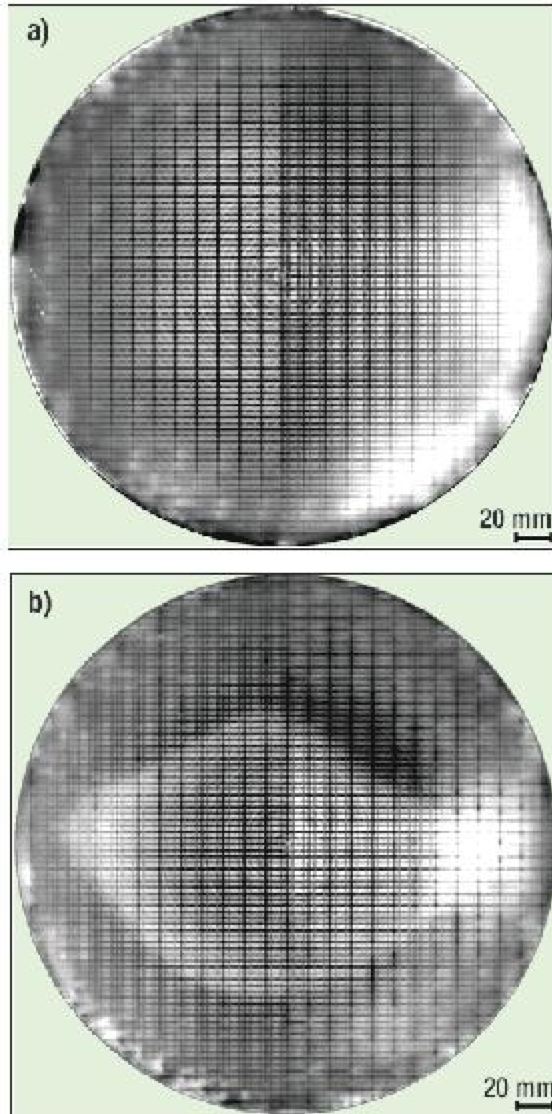

Figure 3. *A reference DRAM back end of line wafer a) and a wafer with poor resist strip b).*

At a major DRAM fab, SPDI inspection was used to evaluate resist strip efficacy [4]. Figures 3a and 3b show two back-end wafers, one reference, the other after a poor resist strip step. The large signature in Fig. 3b shows the organic residue pattern from the incomplete resist strip. The wafers also exhibited different SPDI signatures on the left and right halves due to the presence of Al contamination from open fuses on the left half of the wafers.

	Memory	Logic
Model Inputs: Fab Economics		
Wafer starts per month – ramp start	20,000	10,000
Wafer starts per month – full production	60,000	40,000
Baseline time: 25% to 90% yield (months)	24	24
Devices / 300mm wafer	1480	200
Starting ASP / die	$2	$20
ASP fall rate per month	3%	3%
Model Inputs: NVD Ramp Yield Improvement		
Average # dice per affected wafer per event	8	4
% of wafers affected by each event	100%	8%
# of events during ramp	6	6
Model Inputs: NVD Production Yield Improvement		
Events per year per wet clean bench	2	2
Model Results:		
Peak Improved Yield During Ramp	3.20%	0.90%
Long Term Production Yield Improvement	0.54%	0.54%
Peak Monthly ROI	$1.2m	$0.6m
Cumulative ROI – 2 Years	$19.5m	$8.8m
Cumulative ROI – 5 Years	$25.5m	$20.4m

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New process flows at this fab historically required many specific surface analyses such as ToF-SIMS and AES to optimize resist strip and cleaning sequences. With the SPDI inspection's ability to perform fast scans of experimental wafers, with visual indication of residue locations, the number of analytical scans is greatly reduced and learning cycles accelerated.

Economics of NVD inspection

The previous examples highlight how NVD inspection was able to provide insight to yield issues that traditional optical inspection approaches could not, shaving weeks or months from the time to identify and solve yield problems. This enables a faster yield ramp, allowing a fab to capitalize on the "sweet spot" in device pricing ? the higher average selling prices (ASPs) that accrue to advanced devices in the early months of their manufacture [5]. These economics can be modeled as shown in Table 1. Begin with typical fab economics such as wafer starts, die size, ASP trends, and typical yield ramps; for example, a state-of-the-art 25?90% ramp in 2 years. Model ramp yield events (events that are caught and solved sooner via NVD inspection), with an average percentage of

dice and wafers affected per event. For example, in one DRAM fab an average of 8 dice/affected wafer, on 100% of wafers, were found at 6 steps, whereas the logic charging example described above affected 4 dice/wafer on 1 out of 12 cleans tools, or 8% of wafers affected. Model production events by estimating frequency and impact of NVD events that occur annually per cleans tool.

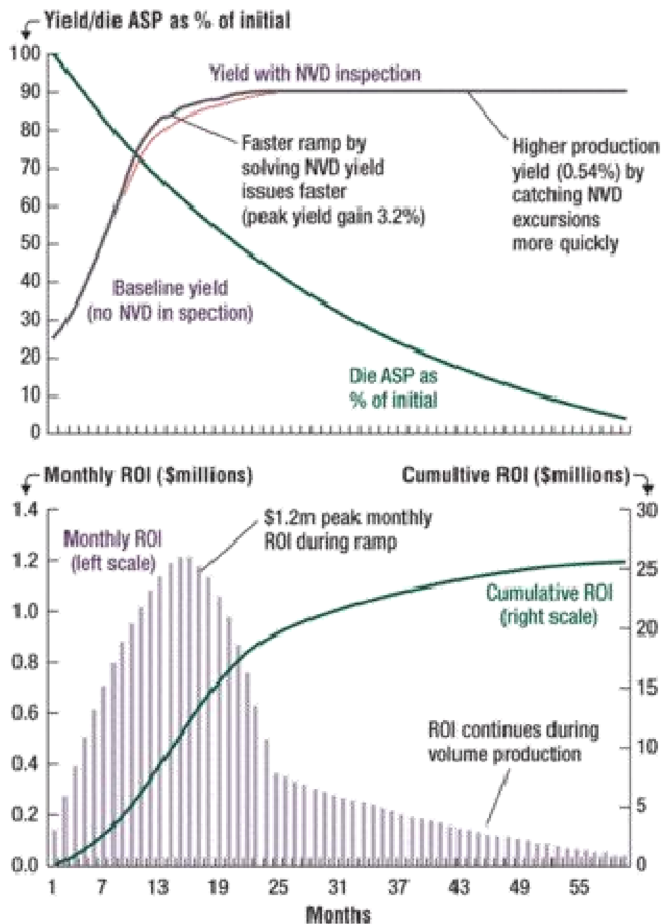

Figure 4. *Modeled 5-year ROI for implementing NVD inspection in a DRAM fab.*
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Figure 4 shows how these values play out over time for the DRAM example. The upper chart shows that the yield at a given point during the ramp is as much as 3.2% higher with NVD inspection. With the relatively high ASPs at that time, fab profitability benefits dramatically ? peaking at over $1.2m per month, as shown in the lower chart. Benefits continue into the production phase, as NVD-related yield excursions are prevented. Cumulatively, the result is a 5-year return on investment (ROI) of $25.5m. The trends for the logic case are similar, with the values shown in Table 1.

Conclusion

The arrival of new semiconductor device structures and processes are giving rise to NVDs, which require new ways of thinking about yield management. Incorporating

inline NVD inspection into a yield management strategy can have a compelling ROI for the fab.

References

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