

VOC & Metallic Contaminant Control For SOI Process Monitoring

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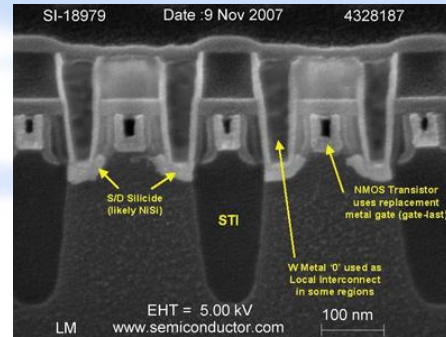
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Introduction: Nanotechnology, SOI and Soitec

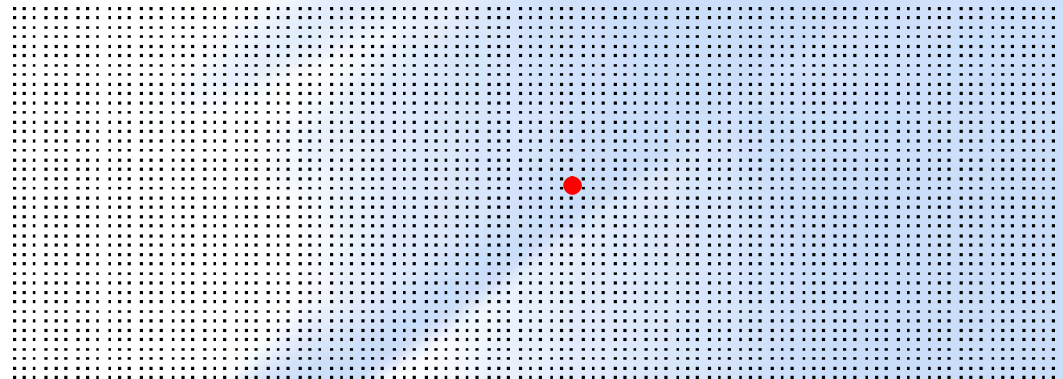
Nanoscale: Not Just Feature Length

Nanoscale usually refers to the lengths of features...



**45nm NMOS Transistor Cross Section
High-k Dielectric and Metal Gates**

...but nanoscale variations in surface condition are critical to manufacturing yield



1 contaminant atom in 4000 on surface = 1.7×10^{11} atoms/cm²
(Density of Surface Atoms on <100> Si Surface is 6.78×10^{14} atoms/cm²)

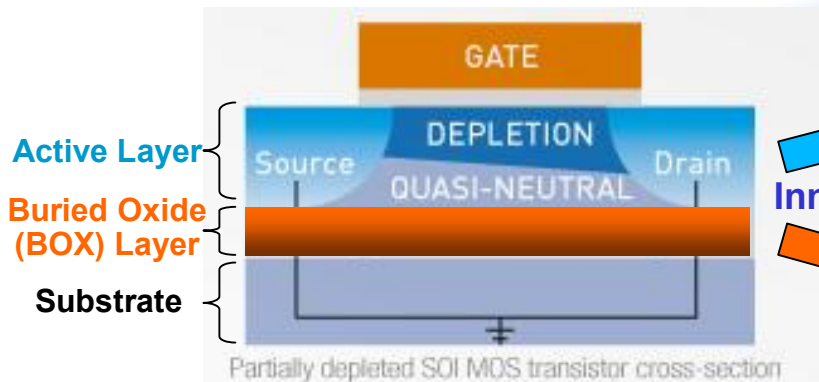
Nanotechnology Commercialization

- **Nanotechnology involves the introduction of significant new materials, structures, and processes**
- **Nanotechnology requires the ability to inspect and control nanoscale characteristics of surfaces over larger-scale areas**
 - **Metal, organic, and inorganic contamination**
 - **Film uniformity**
 - **Surface chemistry**
 - **Atomic scale surface defects/reconstruction**
 - **Surface and dielectric charging**

SOI and Nanotechnology

The Soitec Group's mission is to innovate and industrialize advanced engineered substrates for mobile, high-performance and advanced microelectronic applications.

 **SmartCut SOI Technology**



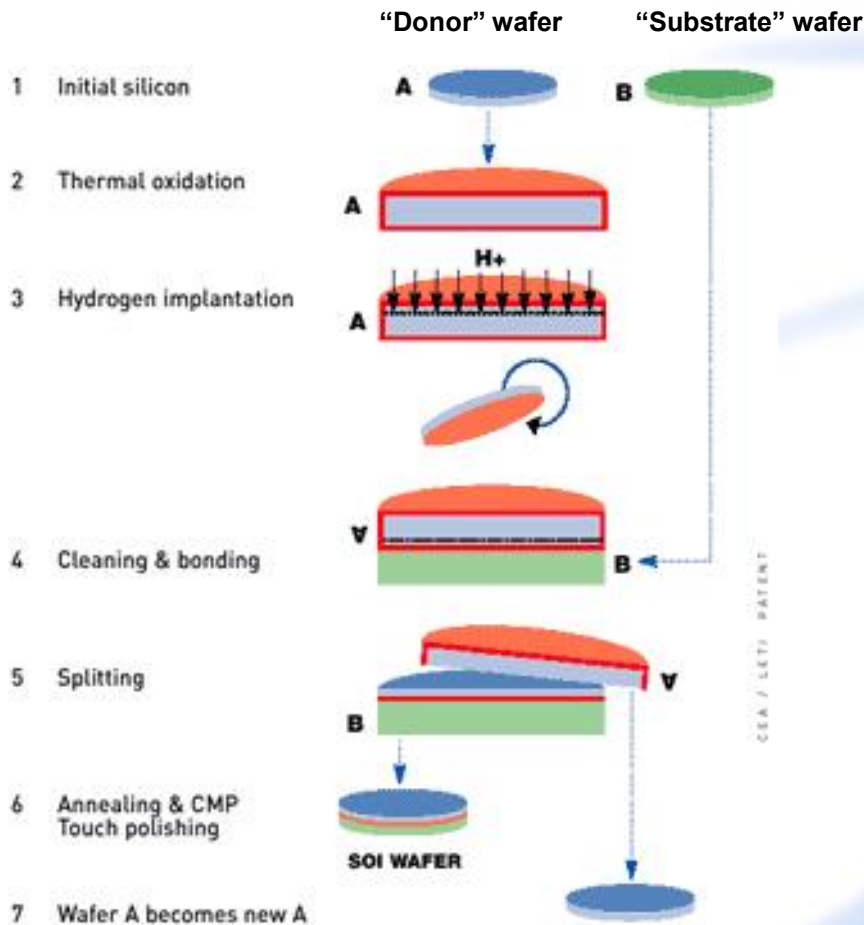
FIVE-YEAR TECHNOLOGY ROADMAP

	2007	2012
Structure engineering	3D integration	
	Patterned / heterogeneous structure	
Active layer engineering	Enhanced performance	
RF / Opto-electronic	GANOI platform	
CMOS	Enhanced mobility	Hybrid orientations
	Strain engineering	Band Gap engineering (Strain Ge, Dual channel)
Buried layer engineering	Device variability control	
	Multi-layer box	
	MugFET integration	
	New functionalities	
	New dielectrics	
	Hybrid SOI	

EC €200 Million NanoSmart Program

The NanoSmart project will expand the Smart Cut "toolbox" into further silicon-related advances, as well as into other materials, particularly in the III-V arena.

Soitec SmartCut Process



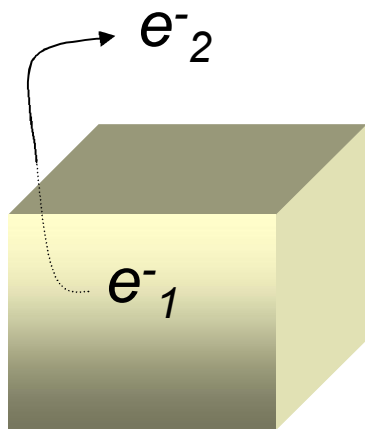
- A buried oxide (BOX) layer is grown atop a Donor Wafer, then this wafer is bonded to a Substrate Wafer
- The Donor Wafer is then split away, leaving the Substrate wafer with the BOX layer and a thin Si layer from the Donor
- Impurities or nonuniformities at any step of the process leads to unacceptable defectivity in the final SOI wafer

ChemetriQ Operating Principles

What are Non-Visual Defects (NVDs)?

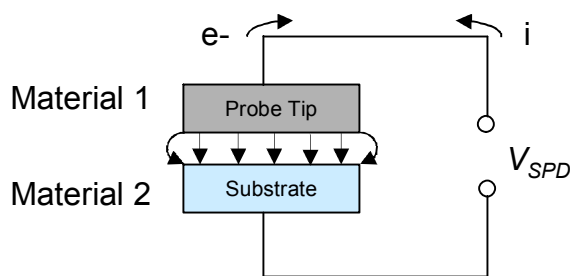
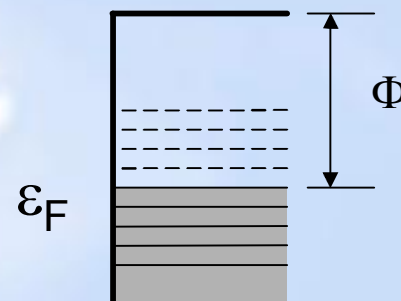
- NVDs do not scatter light and therefore are not detectable using traditional optical inspection tools
- NVDs include:
 - Organic residues
 - Metallic residues
 - Watermarks
 - Process induced charge
- Residues are often less than a monolayer (submonolayer)
- NVDs, like physical defects are yield impacting
- Cleaning and surface preparation are the most repeated steps in the fab
- New NVDs are arising from new cleans, new materials, and tighter specs

ChemetriQ Operating Principle: Fundamentals Based on Work Function Measurement



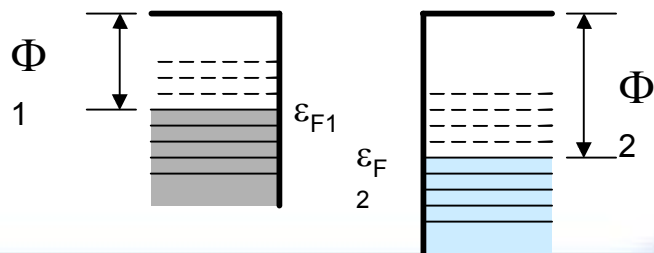
Work Function

the energy (Φ) required to remove an electron from a material's Fermi level (ε_F) to a non-interacting point outside the solid (material).



Surface Potential Difference (SPD)

a method to measure the difference in work function between two materials that are in close proximity and electrically connected.

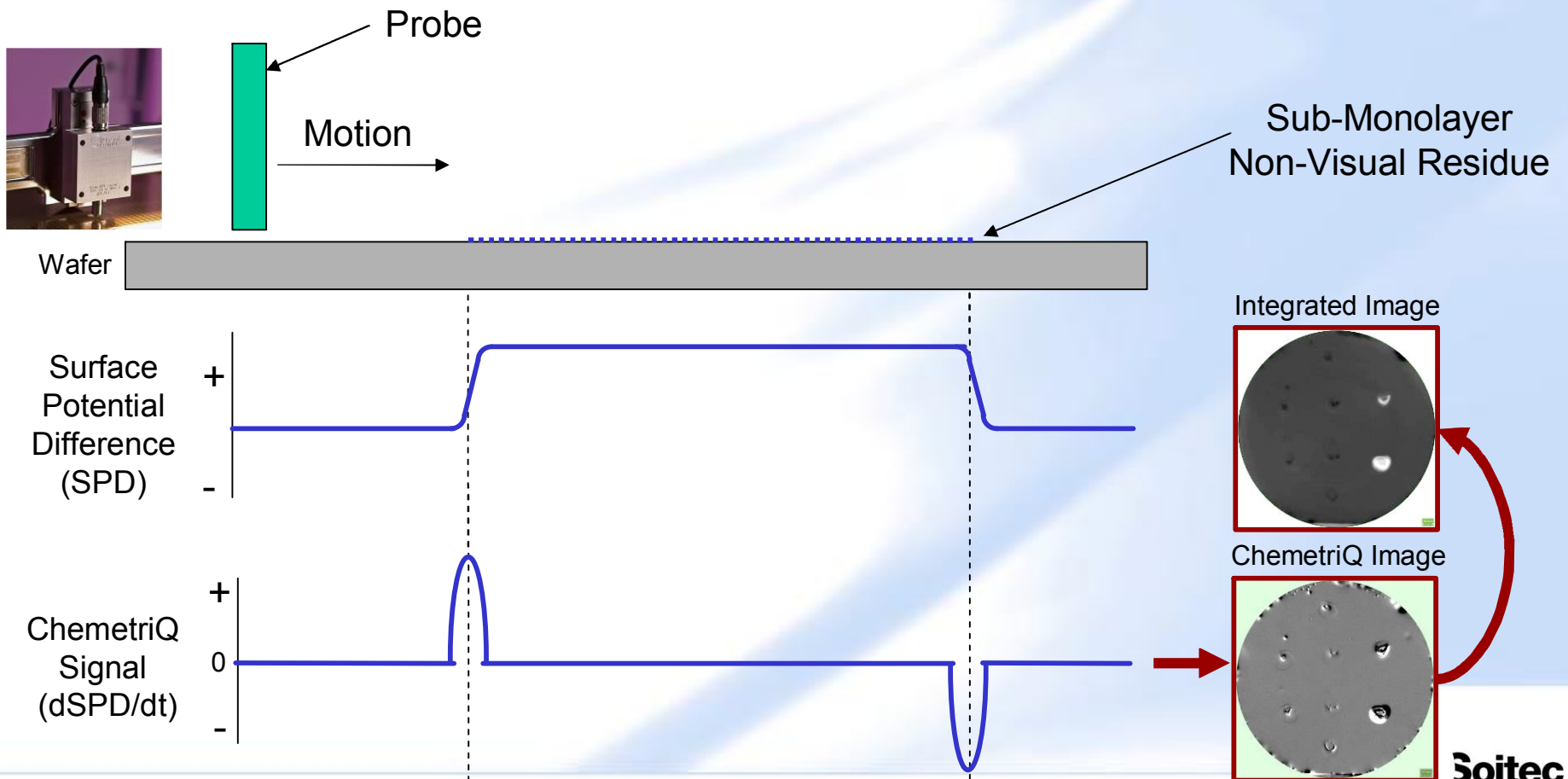


$$V_{SPD} \sim (\Phi_2 - \Phi_1).$$

ChemetriQ Operating Principle:

ChemetriQ Incorporates Differential Work Function Inspection

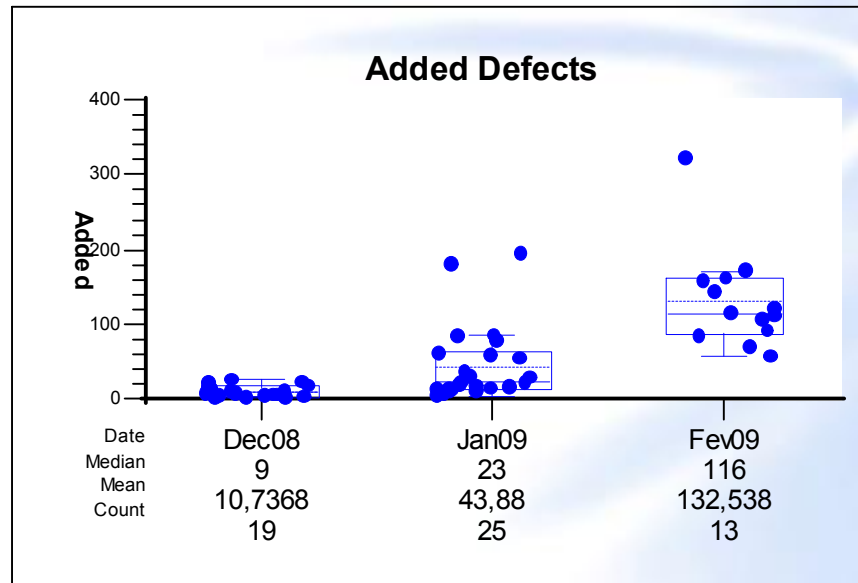
The ChemetriQ Inspection system utilizes a **scanning surface potential difference** system that detects changes in materials and charge on the wafer surface.



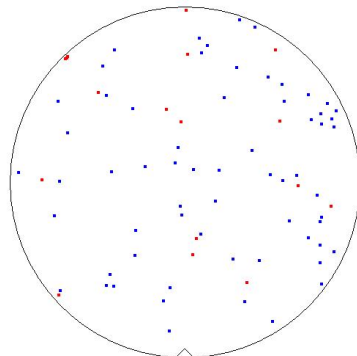
**Process Problem:
Increasing Particle Trend after a Wet Clean Step**

Problem Description - Increasing Particle Defects

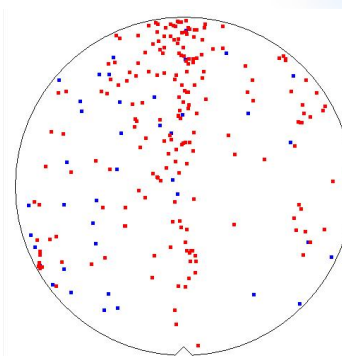
- 50 nm particle levels were increasing after a particular in-line cleaning step



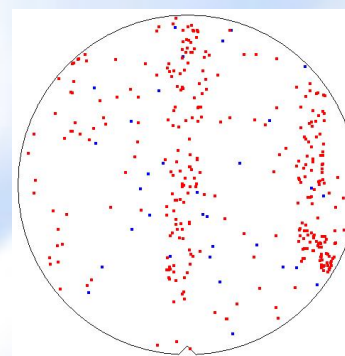
GOAL :
understand the
root cause !



Dec 08
added



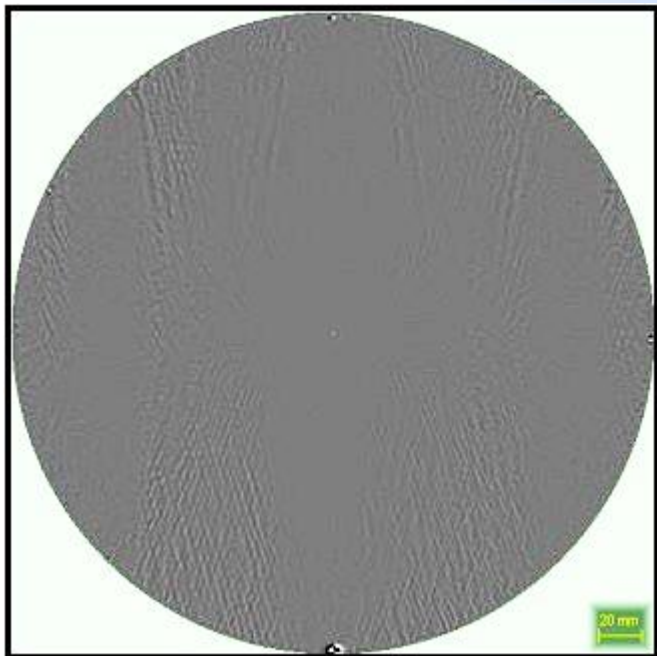
Janv /09
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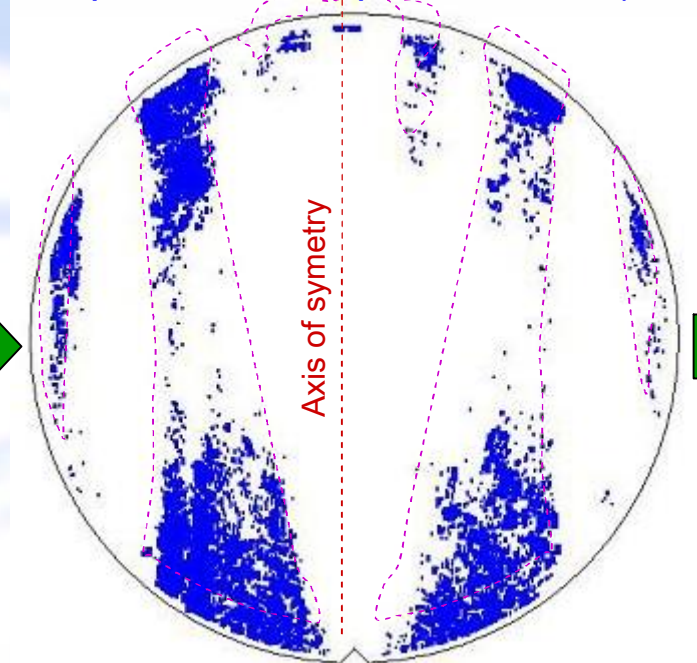
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The ChemetriQ is used to understand defectivity origin

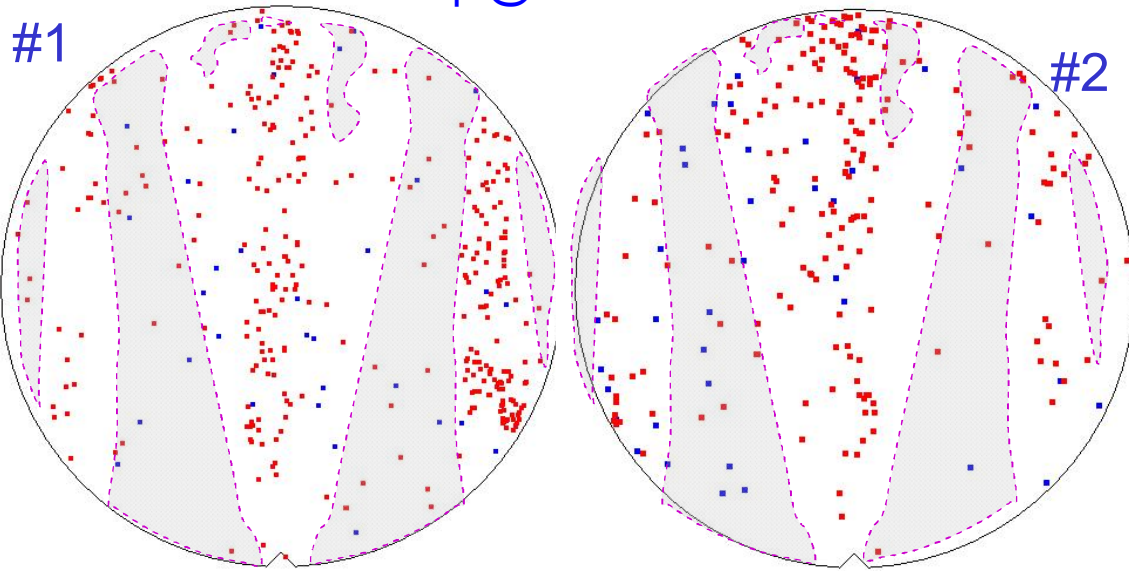
Qcept map after clean :



Qcept stacked maps after clean(18wfrs)

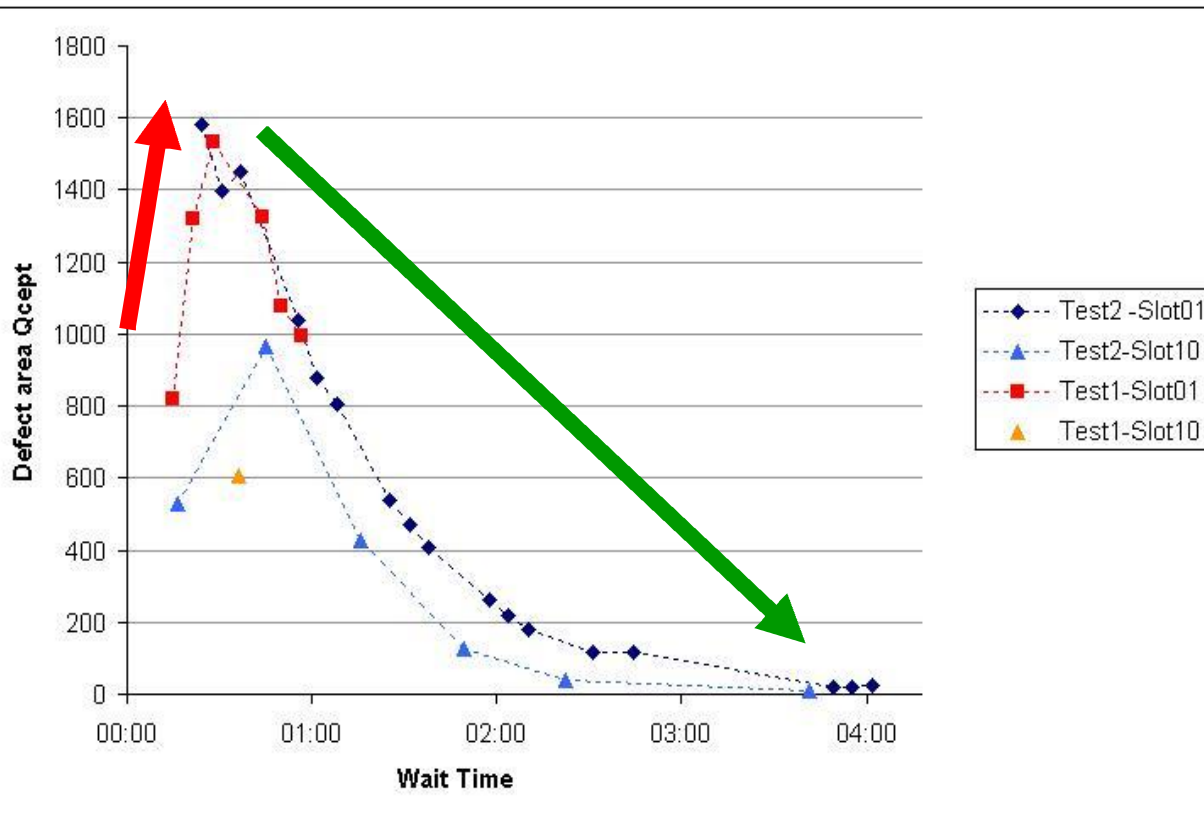


SP2 map @ 50nm after clean



QCEPT pattern matches with particle defectivity seen at 50nm !!

Understanding the Phenomenon



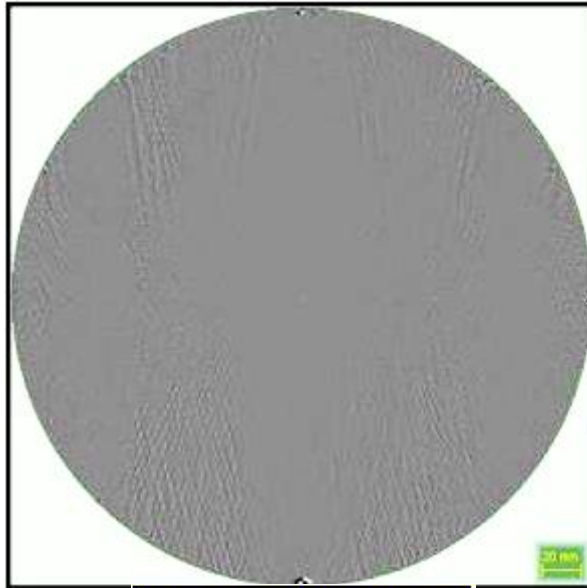
Phase 1 : water layer is uniform; during evaporating water film becomes fragmented; increasing QCEPT defectivity.

Phase 2 : water continues to evaporate until disappearing, returning QCEPT defectivity near 0.

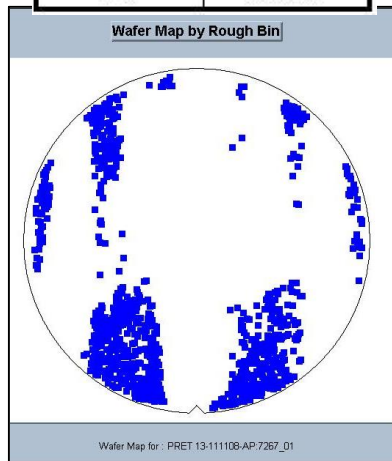
- Defective Area increases at first and then decreases with time
- Hypothesis: The ChemetriQ is detecting water on the wafer surface

Understanding the Phenomenon (cont'd)

Time \approx 1 hour



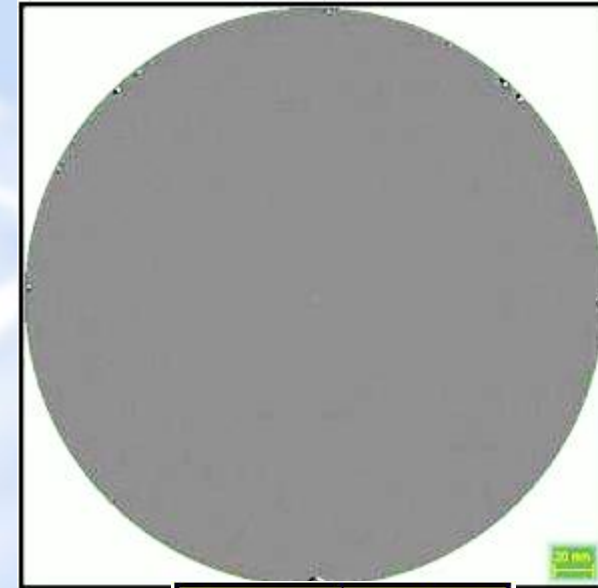
Defect count	Defect area
863	2179.8



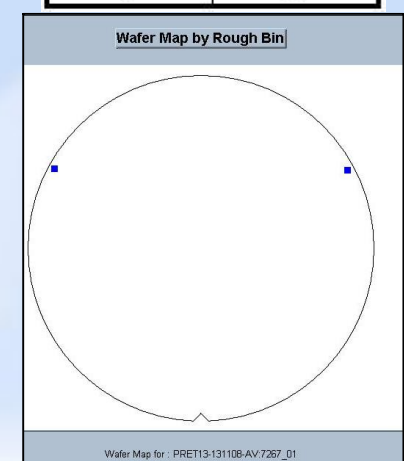
Pattern intensity seen by QCEPT immediately after cleaning increases during the 1st hour then decreases to zero after \sim 4hours



Time \approx 4 hour



Defect count	Defect area
2	4.7



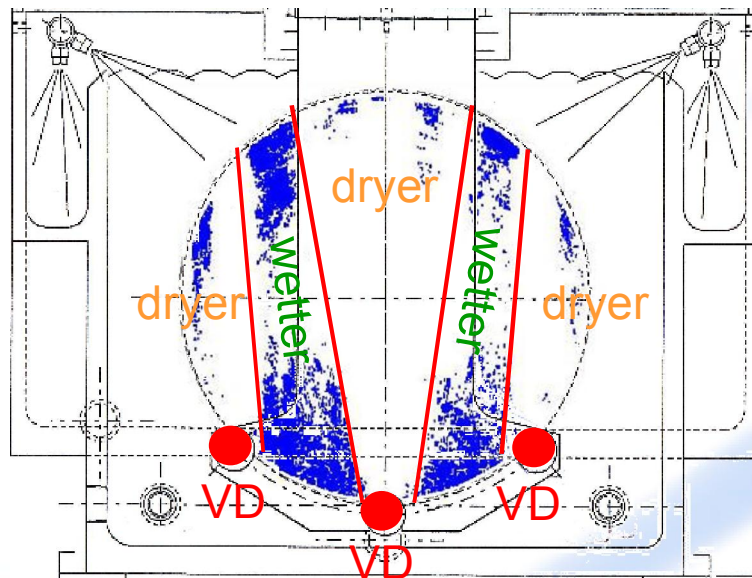
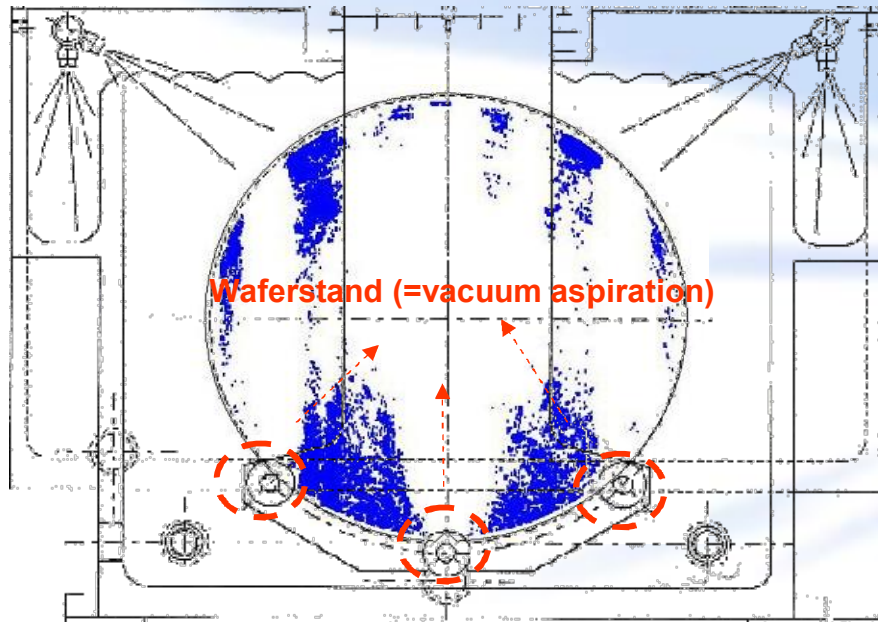
The corresponding defect maps show the decrease in defect counts after 4 hours



Phase 1 : water layer is uniform , during evaporating water film becomes fragmented , increasing QCEPT defectivity.

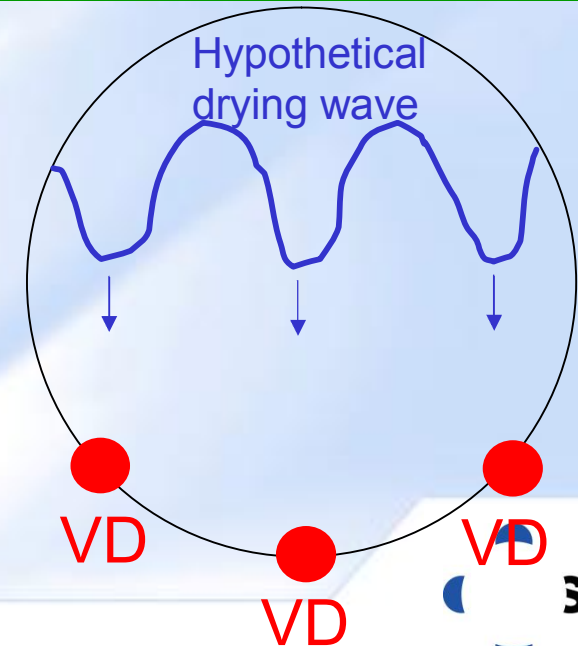
Phase 2 : water continues to evaporate until disappearing, returning QCEPT defectivity near 0.

Link with cleaning tool :



ROOT CAUSE :

- QCEPT pattern seems to be correlated with waferstand & VD (vacuum dry) position
- Area where the drying is faster allows particles to deposit on the wafer
- Corrective action has begun

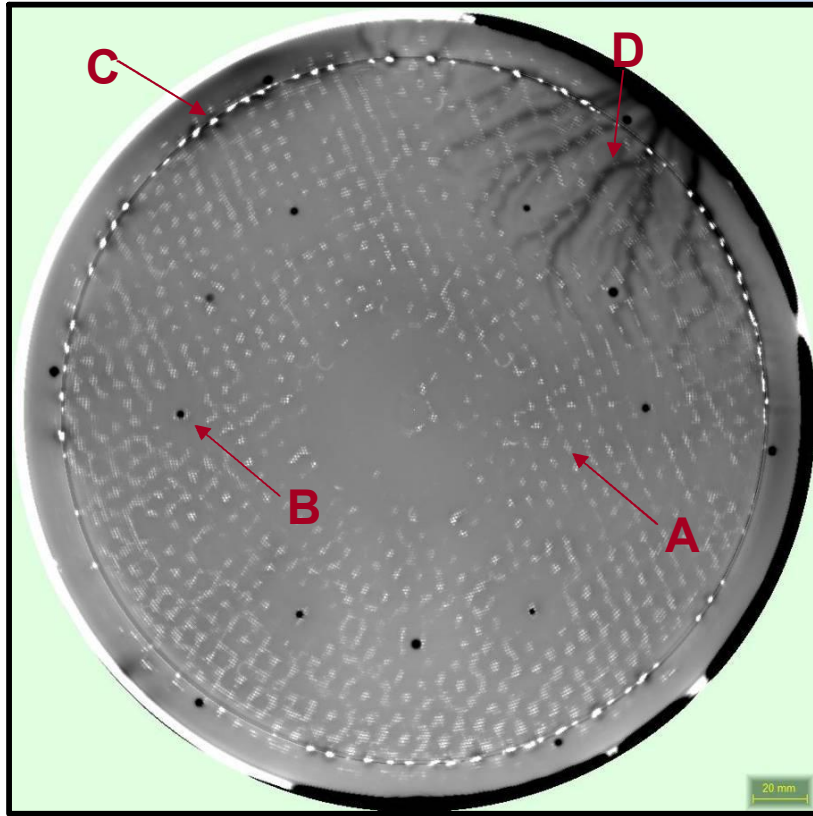


VD = Vacuum Dry

**Process Problem:
Backside Chuck Contamination Defect Sourcing**

Backside Al Contamination

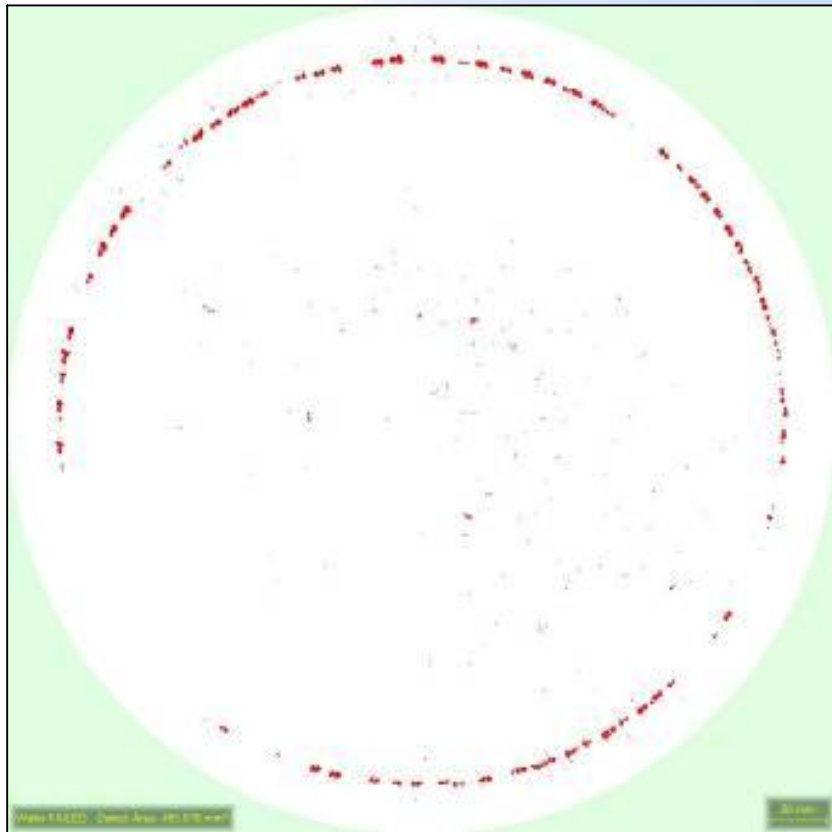
VPD-ICPMS showed Al contamination at $1.2E10$ atoms/cm²



- A particular metrology tool was causing backside Aluminum contamination
- The chuck was suspected and was cleaned many times and the vendor was designing a lower contact chuck
- The image at the left is a ChemetriQ integrated image from a wafer that was placed on the chuck of the metrology tool
- There are 4 distinct regions:
 - Chuck signature (A)
 - Lifter pin signature (B)
 - Electrostatic Ring signature (C)
 - “Dendrite” region (D)

Trace Metals - Backside Al Contamination

ChemetriQ Spatial Signature Provided Critical Piece of Knowledge to Al Source

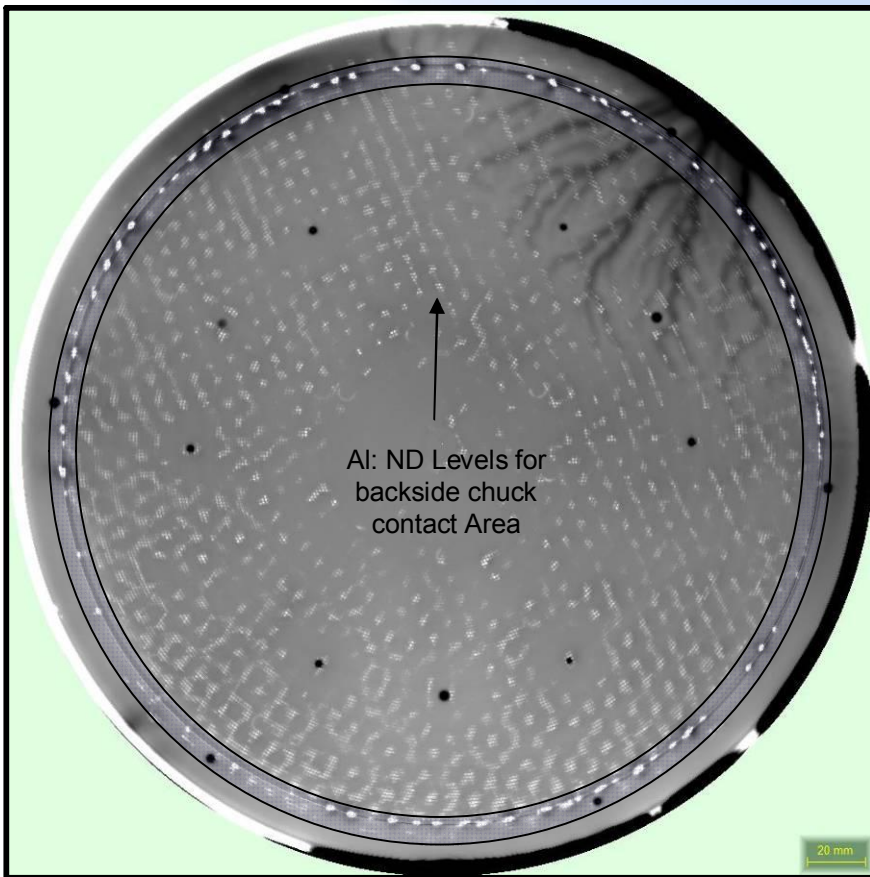


- Positive work function (+WF) defects are generally metallic and negative work function (-WF) defects are generally organic
- So the integrated image was thresholded for +WF defects only
- The resultant defect map showed that the strongest defects were in a ring near the edge of the wafer and not in the center of the wafer from the chuck
- This signature led us to perform TOF-SIMS at the ring signature

The defect map showed that the outer ring was likely the primary source of contamination and not the chuck signature

Trace Metals - Backside Al Contamination

ChemetriQ Spatial Signature Provided Critical Piece of Knowledge to Al Source



Al: $\sim 5E11$ atoms/cm²

Area Adjusted TOF-SIMS:

$1.18E10$ atoms/cm²

VPD/ICPMS:

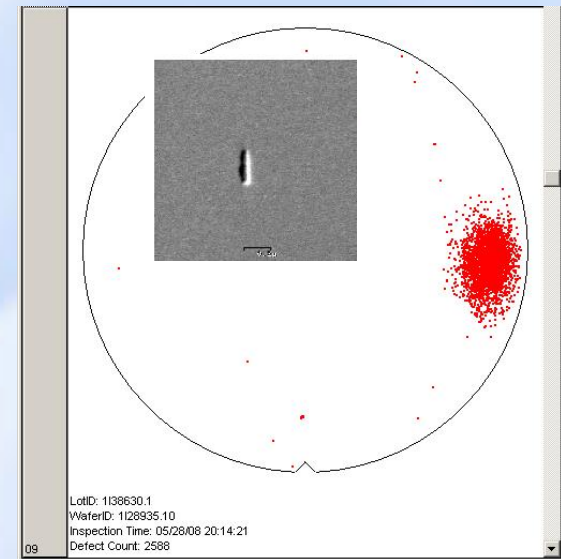
$1.20E10$ atoms/cm²

- The outer ring was analyzed using a TOF-SIMS to identify the element
- Interior reference points of the chuck touch points were also selected with no detectable levels of Al ($<1E8$)
- The outer ring analysis showed an average level of Al contamination at the $5E11$ range, with a maximum reading of $6E12$ atoms/cm²
- The outer ring concentration, when adjusted for area, matched the level of Al from the VPD ICPMS testing
- The proper spatial information provided by the ChemetriQ analysis allowed us to focus on the true source of the contamination

Process Problem: Yield Failure at Final SOI

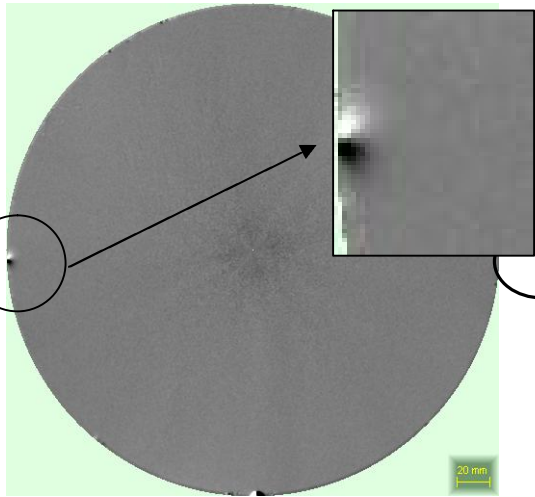
Problem Description - Yield Failure at Final SOI

- **Some SOI wafers were experiencing a yield killing defect at final inspection**
- **This defect was a group of small gouges at the surface located predominately near the 3 o'clock position on the wafer**
- **Traditional inspection techniques could find this defect only at final inspection**
- **The root cause was isolated to a metrology tool that inspected at a step prior to the oxidation step**
- **An inspection was needed to detect this defect at the current process step**

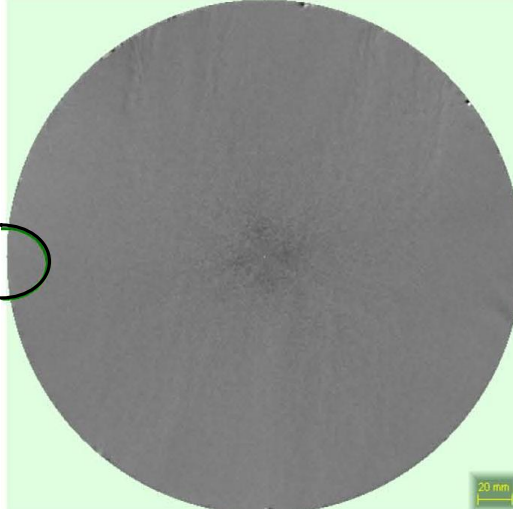


Problem Description - Yield Failure at Final SOI

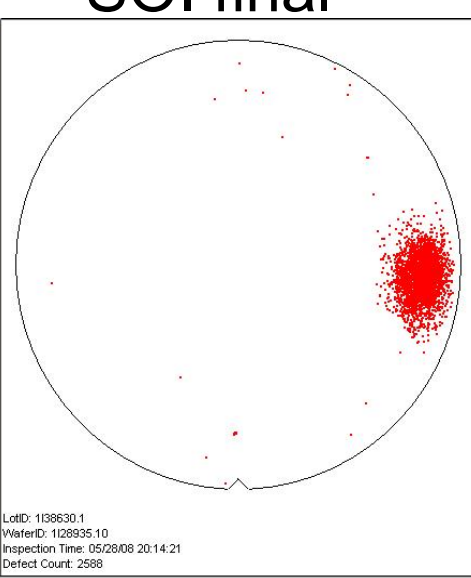
Bad Wafer



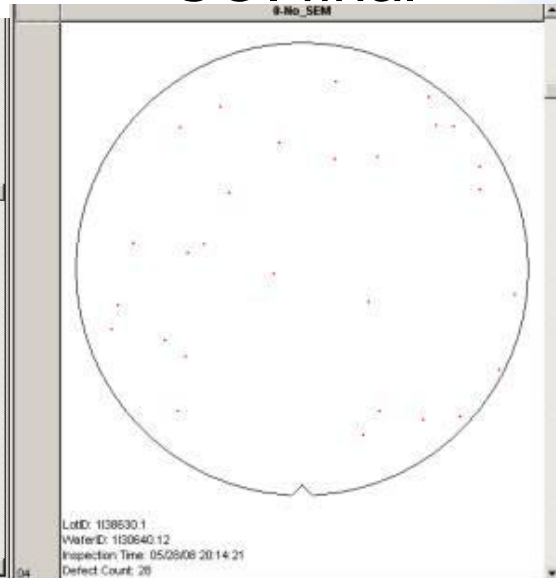
Good Wafer



SOI final



SOI final



- The circled defect on the left is a metallic defect at the very near edge of the wafer
- This matches a touch point from the metrology tool
- This defect at the 9 o'clock position on the SOI donor wafer is the cause of the yield killing defect at 3 o'clock on the final SOI wafer. The donor wafer is flipped and bonded to the base wafer
- A ChemetriQ inspection is now in place as a tool monitor of this metrology tool

Conclusions

Conclusions

- **Nanotechnology requires a greater understanding of the surface conditions in order to ensure yield**
- **In this paper, we presented results using a novel inspection focused on scanning work function**
- **These results provided the ability to better control the surface of the wafer, and thus, improve yields**
 - **Detection of metallic contamination at the wafer edge**
 - **Detection of nonuniform drying leading to particulate issues**
 - **Detection of backside metallic contamination signature**
- **As new processes, new materials and new structures are being introduced, a stronger emphasis on surface inspection will be a requirement**